

output data rates where the video bandwidths are large. This suggests that some form of predetection charge amplification would be desirable to overcome the output circuit noise. We have studied a method of charge and amplification using impact ionization in the high-field region between adjacent CCD gates, and have measured avalanche-induced gain and noise on small charge packets. Of particular interest is that the noise data agrees well with theoretical expectations, and suggests that a CCD imager could be made to operate in a photon-counting mode.

Avalanche multiplication in a surface channel CCD has been reported by Madan *et al.* [1], who gave measurements of gain as a function of clock voltages but no data on noise. Since the usefulness of this process depends on its noise properties, we measured both gain and noise. To minimize competing noise sources we used n-channel buried channel CCD's to avoid surface-state trapping noise and cooled the devices to  $-80^{\circ}\text{C}$  to eliminate dark current noise. The output charge detection circuit on these CCD's is designed for low-noise performance, and in combination with low-noise off-chip signal processing, we routinely obtained noise levels equivalent to 9 electrons rms at a 500-kHz output clock rate.

Avalanche gain in a CCD was induced by application of a large voltage difference ( $\Delta V > 20\text{ V}$ ) between adjacent gates and transfer of an electron packet through the resultant high-field region. Because the high-field region ( $> 10^5\text{ V/cm}$ ) is less than  $1\ \mu\text{m}$  and the probability of an ionization is low, we transferred the packet through the high-field region many times. At  $\Delta V = 26\text{ V}$ , the gain is 2.5 for 200 transfers and the gain per transfer inferred from this is 1.0046.

Neglecting hole ionization, we derived an expression for the avalanche-generated noise which depends on the initial packet size, the noise on the packet before avalanching, and the total gain. For noise measurements we started with packets of 200 to 6000 electrons, used 200 transfers, and varied the voltage difference between 20 and 26 V. The measured data agreed well with the theoretical expression. Using the theory, we show an improvement in the post-detection signal-to-noise ratio for small packets which have undergone avalanche multiplication.

The experimental data also revealed that electrons (other than from impact ionization) were being added to the packet during the gain procedure. These electrons were subsequently avalanched along with the initial packet of interest, giving rise to an "enhanced dark-current" effect. The source of this spurious charge is unknown, but may be the result of hot carriers reaching the oxide-silicon interface and ionizing carriers trapped in interface states.

This work was sponsored by the Department of the Air Force.

- [1] S. K. Madan, B. Bhaumik, and J. M. Vasi, "Experimental observation of avalanche multiplication in charge-coupled devices," *IEEE Trans. Electron Devices*, vol. ED-30, p. 694, 1983.

**IIIA-1 A 2- $\mu\text{m}$  BiCMOS Process Utilizing Selective Epitaxy—**K. K. O, H.-S. Lee, R. Reif, and W. Frank, Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, 60 Vassar St., Rm. 39-529, Cambridge, MA 02139.

The recent advances in bipolar and CMOS technologies have increased the similarities and the complexity of processing requirements of both technologies to a point where merging these two technologies has become a viable option. This paper describes a BiCMOS process which incorporates a high-performance n-p-n bipolar structure with a cutoff frequency ( $f_T$ ) of 5 GHz and an isolated nonoptimized vertical p-n-p bipolar structure to a 2- $\mu\text{m}$  twin-well CMOS process with poly-to- $\text{n}^+$  capacitors. These high-performance structures are incorporated with only 2 additional masking steps without affecting the performance of the NMOS and

PMOS transistors of the original CMOS process. The device characteristics of the vertical n-p-n and p-n-p transistors, as well as the NMOS and PMOS transistors, will also be described.

The vertical n-p-n bipolar structures are fabricated in an arsenic-doped selective epitaxial layer deposited on  $\text{n}^+$  subcollectors (located in p-wells) after the LOCOS field oxidation step of the CMOS process. The base-collector junctions of the vertical n-p-n transistors are dielectrically isolated to minimize the parasitic capacitance and to increase the junction breakdown voltage. The dielectrically isolated junction structure is formed by exposing the base-collector junction using a mesa etch, and passivating the exposed junction using a thermal oxidation step. The isolation structure is completed by depositing a boro-phospho-silicate glass (BPSG) layer on top of the thermal oxide layer during the first interlevel dielectric deposition step of the CMOS process. The mesa structure allows simultaneous formation of  $\text{n}^+$  emitters and collector plugs during the  $\text{n}^+$  source-drain implantation step without increasing the collector series resistance. The mesa etch also removes the defective regions at the edges of the selective epitaxial layer to form defect-free base-collector junctions. In addition, the sloped mesa structure alleviates the metal step coverage problem.

The vertical p-n-p structures are formed by depositing the arsenic-doped selective epitaxial layer on p-wells. The p-wells are used as collectors, and  $\text{p}^+$  emitters are formed during the  $\text{p}^+$  source-drain implantation step. If the starting wafer is an n-n $^+$  epitaxial wafer, the vertical p-n-p transistors are junction-isolated.

The device characteristics for the NMOS and PMOS transistors are similar to those of the MOS transistors of the original CMOS process. The  $LV_{CEO}$  and  $BV_{CBO}$  of the vertical n-p-n transistors are 9 and 30 V, respectively. The current gain  $h_{FE}$  of the vertical n-p-n transistors is 70 and is flat for over 3 decades of collector current. The Early voltage is 40 V. The  $LV_{CEO}$  and  $BV_{CBO}$  of p-n-p transistors are greater than 20 V. The  $h_{FE}$  of the vertical p-n-p transistors is 70 and the Early voltage is approximately 300 V. The high breakdown voltage and the high Early voltage of the vertical p-n-p transistors are due to an extremely low collector doping concentration ( $2 \times 10^{15}\text{ cm}^{-3}$ – $3 \times 10^{15}\text{ cm}^{-3}$ ). For the same reason, the collector series resistance of the vertical p-n-p structures is high and current driving capability is limited. However, the vertical p-n-p structures still have a higher current driving capability per area than the NMOS transistors. Despite the high collector series resistance, the cutoff frequency  $f_T$  of the vertical p-n-p transistors is expected to be on the order of hundreds of megahertz.

This work was supported by the Semiconductor Research Corporation under Contract 87-SP-080.

Student paper.

**IIIA-2 A Novel Germanium Implanted Salicide Technology for CMOS VLSI—**James R. Pfister and Robert Yeagain, Advanced Products Research and Development Laboratory, Motorola, Inc., 3501 Ed Bluestein Blvd., Austin, TX 78721.

A novel salicided twin-tub CMOS process using germanium implantation has been developed and characterized. Implantation of  $\text{n}^+$  and  $\text{p}^+$  dopants after titanium salicidation are employed to fabricate devices with low junction leakage and good short-channel effects.

Salicidation of shallow junctions has been shown to result in increased leakage current which can be aggravated by the isolation edge pull back for a LOCOS based isolation [1]. Additional source-drain implantation after titanium deposition either before [1] or after silicidation [2] have been proposed to minimize these problems. In this process, germanium implantation is performed prior to titanium salicidation while phosphorus and boron are post-implanted to form the shallow  $\text{n}^+$  and  $\text{p}^+$  regions, respectively.