

A High-Speed CMOS Dual-Phase Dynamic-Pseudo NMOS ((DP)²) Latch and Its Application in a Dual-Modulus Prescaler

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Abstract—A high-speed dual-phase dynamic-pseudo NMOS ((DP)²) latch using clocked pseudo-NMOS inverters is presented. Compared to the conventional D-latch, this circuit has a higher maximum operating frequency and consumes lower dynamic power at a given operating frequency. The latch has been demonstrated by utilizing it in the synchronous counter section of a dual-phase dual-modulus prescaler implemented in a 0.8- μm CMOS process. The maximum operating frequency for the prescaler at 3 V supply voltage is 1.3 GHz, while the power consumption is 9.7 mW. This power consumption is significantly lower than those of the previously reported prescalers implemented in 0.8- μm CMOS processes. The 9.7-mW power consumption at 1.3 GHz also compares favorably to the 24-mW power consumption of the 1.75-GHz prescaler using MOS current mode latches implemented in a 0.7- μm CMOS process. A 25% reduction of the maximum operating frequency for a $\sim 60\%$ reduction of the power consumption should be a useful tradeoff.

Index Terms—D-latch dual-modulus prescaler, dual-phase dynamic pseudo-NMOS latch ((DP)²), MOS current mode logic (MCML), pseudo-NMOS inverter, synchronous counter.

I. INTRODUCTION

A DUAL modulus prescaler is a critical part of phase-locked loop frequency synthesizers [1], [2]. One of the speed limitations of prescalers is the maximum operating frequency of the synchronous counter section [1], [3], [4]–[6]. In this paper, to increase the maximum operating frequency of the synchronous counter section, a high-speed CMOS dual-phase dynamic-pseudo NMOS ((DP)²) latch is proposed [5] and demonstrated in a dual-phase dual-modulus prescaler fabricated in a 0.8- μm CMOS process. It consists of two clocked pseudo-NMOS inverters [5], [7]. This inverter has one fewer lower-speed PMOS transistor than a conventional clocked inverter [8], which reduces the total parasitic capacitance and thus the dynamic power consumption. This removal of a PMOS transistor also decreases the resistance through which the circuit nodes are charged and discharged, and this improves the speed performance. Compared to latches using MOS current mode logic (MCML) [3], [9], a single-ended (DP)² latch generates more switching noise. On the other hand, the (DP)² latch is smaller and easier to design since it only

needs six transistors versus 20 transistors in an MCML latch [3]. The MCML circuits also need an additional bias signal [3] and a generator for the signal which consumes additional area and power. (DP)² latches which are relatively easy to design should be useful for numerous applications due to their smaller area, improved speed performance, and reduced dynamic power consumption.

II. DESIGN OF THE DUAL-PHASE DYNAMIC-PSEUDO NMOS ((DP)²) LATCH

A clocked pseudo-NMOS inverter is shown in Fig. 1(a). In this inverter structure, one of the two lower-speed PMOS transistors in a conventional clocked inverter [8] has been eliminated. By cascading two of these clocked pseudo-NMOS inverters, a higher-speed (DP)² latch shown in Fig. 1(b) is constructed. When CLK = 0 and D = 0, \overline{Q} = 1 and Q is in the high impedance or hold state. When CLK = 1 and D = 0, \overline{Q} is in the high-impedance state while Q is a complement of the \overline{Q} . Thus, at the end of one clock cycle, input signal (D) is passed to the output just like in a conventional D-latch. The simulation results using a 0.8- μm CMOS process show that when the capacitive loads for CLK and $\overline{\text{CLK}}$ are kept the same, the maximum operating frequency of a divide-by-two counter using the (DP)² latch is 1.92 GHz which is 1.67 times higher than 1.15 GHz of a divide-by-two counter using a conventional D-latch. In Fig. 1(b), when CLK is low and D is high, all three transistors of the first stage are turned ON and the low output voltage is determined by a “resistive voltage divider” formed by the transistors. Because of this, the static power consumption is not zero for this circuit. If properly designed, when the output of the inverter is low, the PMOS transistor M0 is in the saturation region, while the NMOS transistors M1 and M2 are in the linear region. The low \overline{Q} behaves like the low output voltage of a pseudo-NMOS inverter given by the following expression:

$$V_{\overline{Q}L} = V_{DD} - V_{TN} - \sqrt{(V_{DD} - V_{TN})^2 - \frac{\beta_P}{\beta_{NT}}(V_{DD} + V_{TP})^2} \quad (1)$$

where V_{DD} is the power supply voltage; V_{TP} and V_{TN} are the threshold voltages of PMOS and NMOS transistors, respectively; β_{NT} is the effective transconductance parameter of NMOS transistors M1 and M2 and β_P is the transconductance parameter of PMOS transistor M0. This is the reason for the inclusion of “pseudo-NMOS” in the name of the circuit. β_{NT} is related to the transconductance parameters, β_{N1} and β_{N2} ,

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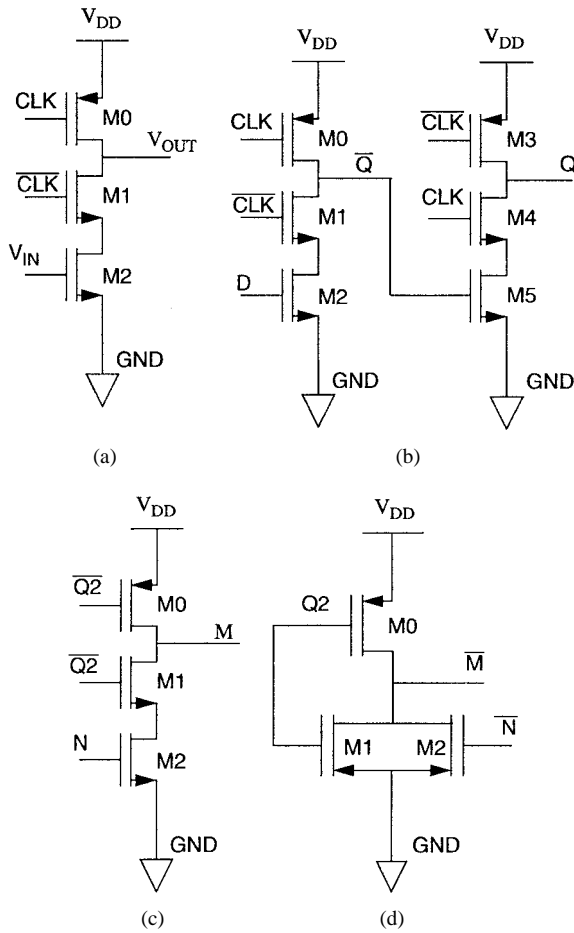


Fig. 1. (a) Schematic of a pseudo-NMOS dynamic inverter. (b) A schematic of a $(DP)^2$ latch. By cascading two pseudo-NMOS dynamic inverters, a higher speed $(DP)^2$ latch is constructed. (c) and (d) Schematics of the NAND and NOR gates. Taking advantage of the dynamics of the prescaler, the NAND and NOR gates with reduced input capacitances have been implemented.

of the NMOS transistors M1 and M2 by (2)

$$\beta_{NT} = \frac{\beta_{N1}\beta_{N2}}{\beta_{N1} + \beta_{N2}}. \quad (2)$$

In actual design situations, the desired V_{QL} is known, and the ratio between β_p and β_{NT} should be adjusted to obtain the V_{QL} . Equation (1) can be rearranged into (3) to express the ratio between β_p and β_{NT} as a function of V_{DD} , V_{TN} , V_{TP} , and V_{QL}

$$\frac{\beta_p}{\beta_{NT}} = \frac{(V_{DD} - V_{TN})^2 - (V_{DD} - V_{TN} - V_{QL})^2}{(V_{DD} + V_{TP})^2}. \quad (3)$$

From the above expressions, in order that $V_{QL} \approx 0$, either the width of the PMOS transistor M0 should be decreased or the widths of the NMOS transistors M1 and M2 should be increased. Reducing the width of M0 increases the rise time t_r , which degrades the speed performance of the inverter. Obviously, there is a tradeoff between the speed and noise margin.

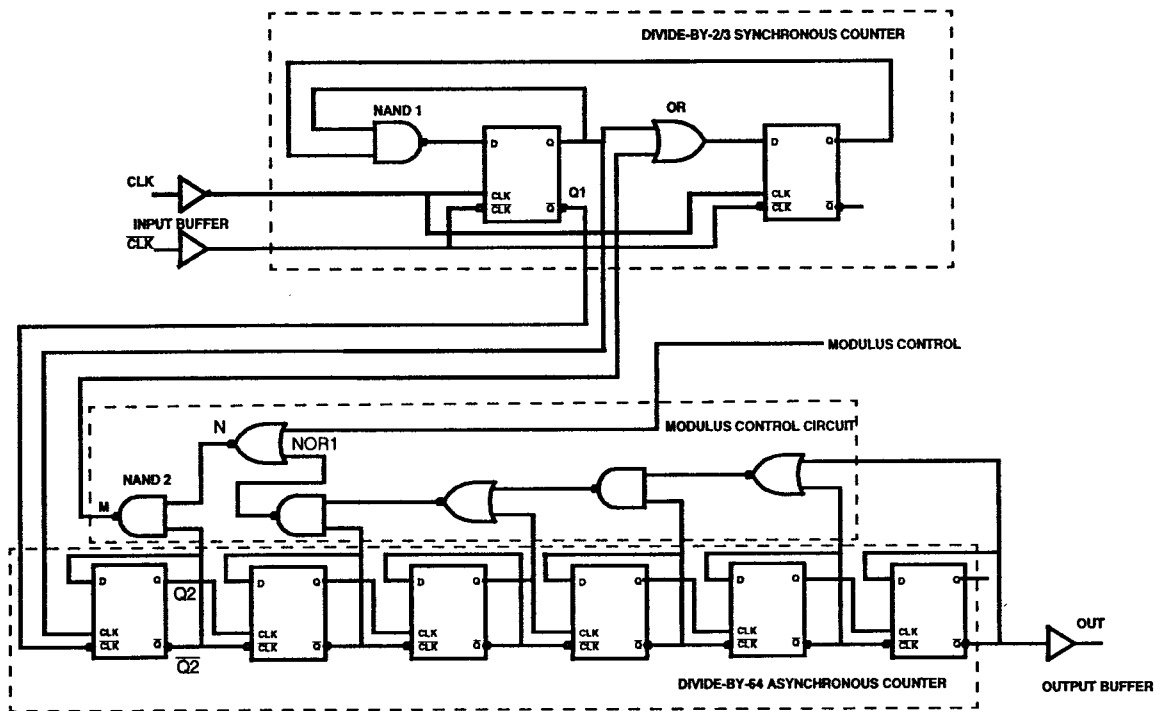
A similar voltage divider is formed when CLK and \bar{Q} are high except that now all three transistors of the second dynamic inverter are turned ON. The $(DP)^2$ latch passes a "strong" high output but does not pass a "strong" low output.

It is faster than the conventional D -latch because it has just one slower PMOS transistor in each of the clocked inverters. Additionally, the input capacitance of the inverters is lowered since only an NMOS transistor is connected to the input. These improve the speed performance and lower the dynamic power consumption. These, however, are accompanied by an increase of the static power consumption. Because of this, the circuit may not be attractive for low-speed circuit design. But, it is well suited for the high-speed applications where the circuit is switching all the time. In such applications, the dynamic power dissipation due to the continuous switching at high frequencies dominates, and the added static power dissipation is not significant.

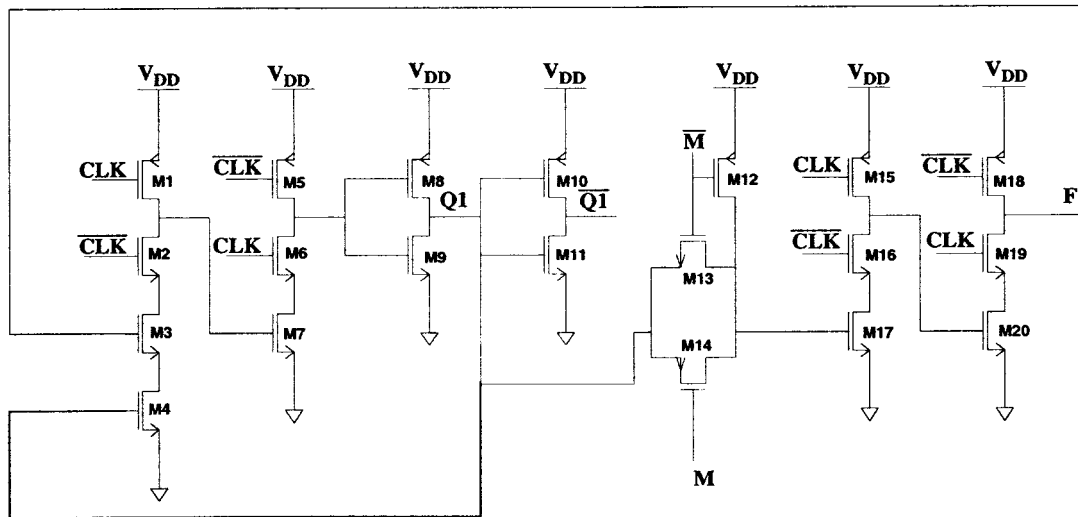
III. DESIGN OF THE DUAL-PHASE DUAL-MODULUS PRESCALER

A block diagram of the divide-by-128/129 dual modulus prescaler is shown in Fig. 2(a) [5], [8]. The prescaler consists of three main parts: a synchronous counter, an asynchronous counter and a modulus control logic circuit. To decrease the dynamic power consumption, a divide-by-two or three synchronous counter shown in Fig. 2(b) is used instead of a conventional divide-by-four or five synchronous counter [1], [8]. A concern for using a divide-by-two or three for synchronous counter is a smaller operation margin for the modulus control logic circuit compared to the prescalers using a divide-by-four or five counter when divisions-by-129 (or a division-by-three for the synchronous counter) are desired [10].

For the synchronous counter to divide by three, a low-level signal of Q1 in Fig. 2(b) should be passed to the second latch and fed back to the gate of M3. This happens only when both M and Q1 are low. The high-to-low transition of M is delayed by t_d from the high to low transition of Q1 and in normal operation, for the circuit to operate properly, t_d must be less than two clock cycles for a divide-by-two or three synchronous counter and less than four clock cycles for a divide-by-four or five synchronous counter. These limits are commonly referred as the operation margin [10]. The prescaler fails to divide by three when t_d becomes too close to the operation margin. When the input frequency is sufficiently increased, t_d could become longer than two clock cycles. As a matter of fact, it could become three or four times the clock period or higher. If Q1 is low after the high-to-low transition of M, even though this transition has occurred after $t_d > \text{two times the clock period}$, provided that the synchronous counter is sufficiently fast, a low signal of Q1 can be passed to the second latch and fed back to the gate of M3 for a division-by-three operation. By exploiting this, the speed requirement of the modulus control logic circuit can be relaxed so that the maximum operating frequency of the prescaler is limited by the maximum operating frequency of the synchronous counter. This can only be done over a set of frequency ranges. A frequency range in which the division-by-three functions properly can be chosen as needed. The design technique for this is discussed in detail in [1] and [8]. This technique of course requires the operating frequency range of



(a)



(b)

Fig. 2. (a) Block diagram of the divide-by-128/129 dual modulus prescaler. The prescaler consists of three main parts: a synchronous counter, an asynchronous counter, and the modulus control logic circuit. (b) Schematic of the divide-by-two or three synchronous counter including two $(DP)^2$ latches.

the prescaler be restricted. The asynchronous counter consists of six cascaded T-latches for division-by-64.

To increase the speed of the synchronous counter, two $(DP)^2$ latches have been used in the design. The design value of V_{QL} (or $V_{\bar{Q}L}$) in these $(DP)^2$ latches is ~ 0.3 V. The NAND1 in Fig. 2(a) and the first clocked inverter in the first $(DP)^2$ latch are coalesced (M2–M4) [1], [10]. This decreases the number of gates, thus reducing power consumption and increasing the speed performance. In addition, the pass transistor logic [1], [10] is used to implement the OR gate (M12–M14). When the modulus control logic output M is one, the counter divides by two and when M is low, the counter divides by three.

In Fig. 2(b), M is the output of the NAND2 gate shown in Fig. 2(a). For proper operation of the OR gate in the synchronous counter, both M and \bar{M} are required. To generate \bar{M} , an inverter could be used but this would introduce an extra delay and increase the total delay (t_d) through the modulus control logic circuit. Instead, the Q and \bar{Q} outputs of the T-latches [1], [5] in the asynchronous divide-by-64 counter are used to drive a NOR and NAND gate pair to generate M and \bar{M} .

Taking advantage of the dynamics of the prescaler, NAND and NOR gates with reduced input capacitances shown in Fig. 1(c) and (d) have been implemented. These circuits ex-

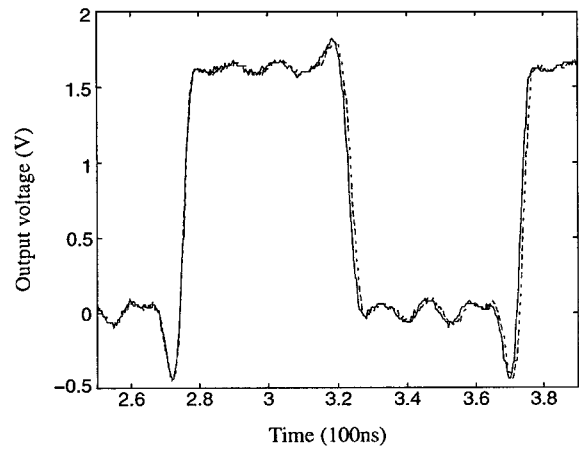
plot the fact that the transitions of the synchronous counter from division-by-three to division-by-two are solely controlled by Q2 and $\overline{Q2}$. $\overline{Q2}$ is the inverted output of Q2 which is the output of the first asynchronous stage [Fig. 2(a)]. N which is the output of the NOR1 gate in Fig. 2(a) remains at high during this transition, while the inverted output of N (\overline{N}) remains at low. Because of this, the pull-ups associated with \overline{N} and N are not required for this transition. This enables the width of M0 in the NOR and NAND gate to be reduced. This in turn decreases the input capacitances of the gates thus reducing the load for Q2 and $\overline{Q2}$ and speeding up the first asynchronous stage.

IV. PERFORMANCE EVALUATION

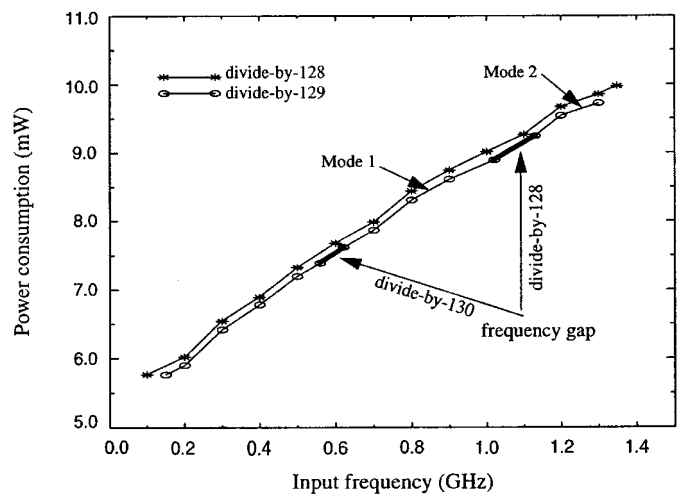
The area of the fabricated prescaler including the input and output buffers is $\sim 260 \mu\text{m} \times 320 \mu\text{m}$. This prescaler was characterized using an HP 8341A to generate the input clock signals. The in-phase and out-of-phase clock signals were generated using a power splitter with 0° and 180° phase-shifted outputs. The input clock signals are terminated using two on-chip $50\text{-}\Omega$ polysilicon resistors.

The maximum input frequency ($f_{in,max}$) for the circuit at 3-V supply voltage is 1.3 GHz, and this is limited by the divide-by-129 operation. This frequency is much higher than 620 MHz at 3 V of the previously reported dual modulus prescaler using a conventional latch implemented in a $0.8\text{-}\mu\text{m}$ CMOS process [11]. Fig. 3(a) shows divided-by-128 and divided-by-129 output waveforms at 1.3 GHz. The output swings from zero to 1.5 V, because the supply voltage of the output buffer was set to 1.5 V to reduce the power rail bounce problem during the measurements. The maximum divide-by-128 operating frequency of this prescaler is 1.34 GHz, which is also the highest operating frequency of the synchronous counter or the $(DP)^2$ latches. The fact that the maximum divide-by-128 and divide-by-129 frequencies are close suggests that the synchronous counter is the speed bottleneck near 1.3 GHz.

Fig. 3(b) shows plots of the power consumption versus input frequency at $V_{DD} = 3.0$ V for division by 128 and 129. The power consumption increases linearly with frequency due to an increase in the dynamic power consumption. At the highest mode-1 operating frequency of 1.02 GHz, the prescaler consumes 8.9 mW (the power consumption of the output buffer is negligible). To operate the previously reported prescaler [11] at 1.02 GHz, the minimum supply voltage should be ~ 4.25 V with corresponding power consumption of ~ 17 mW. This is 1.9 times higher than that of the prescaler described in this paper. At 1.3 GHz, the power consumption of the prescaler is 9.7 mW. This is also significantly lower than ~ 30 mW at 1.3 GHz of another previously reported $0.8\text{-}\mu\text{m}$ CMOS prescaler [7]. The maximum operating frequency of this prescaler is lower than the 1.75-GHz CMOS prescaler utilizing the MCML latches [2]. However, using these results to compare the speed performance of $(DP)^2$ and MCML latches is not straight-forward, because the 1.75-GHz prescaler employs a different prescaler architecture and is fabricated in a $0.7\text{-}\mu\text{m}$ process with a 2-nm thinner gate oxide layer, which should have higher speed performance than the process used



(a)



(b)

Fig. 3. (a) Waveforms of the divide-by-128 and divide-by-129 outputs at 1.3 GHz. The output swings from zero to 1.5 V because the supply voltage of the output buffer was set to 1.5 V to reduce the power rail bounce problem during the measurements. (b) Measured power consumption for division by 128 and 129 versus operating frequency at $V_{DD} = 3$ V. The power consumption increases linearly with frequency due to an increase in the dynamic power consumption.

for this work. The 9.7-mW power consumption at 1.3 GHz compares favorably to the 24-mW power consumption at 1.75 GHz for the $0.7\text{-}\mu\text{m}$ CMOS prescaler. A 60% reduction of power consumption for a 25% reduction in the maximum operating frequency should be useful. This plot also shows the operating frequency ranges for different modes and the gaps between the modes discussed in [1]. The prescaler fails to divide by 129 between 570 and 610 MHz, and between 1.03 and 1.12 GHz. However, for wireless applications in which the band of interest is restricted to over a few tens of megahertz [12], this technique should be well suited.

V. CONCLUSIONS

A 3-V divide-by-128/129 dual-phase dual-modulus prescaler implemented in a $0.8\text{-}\mu\text{m}$ CMOS process is used to demonstrate the performance of $(DP)^2$ latch. This latch has higher speed performance and smaller layout area, and consumes less dynamic power compared to latches using conven-

tional clocked inverters. It has been used in the synchronous counter section of a prescaler to increase its maximum operating frequency. The prescaler operates up to 1.02 GHz in mode 1 [1] with a 3.0-V supply and consumes 8.9 mW; and when in mode 2 [1], the maximum frequency increases to 1.3 GHz with power consumption of 9.7 mW. At a given operating frequency, this prescaler consumes significantly lower power than the previously reported prescalers implement in 0.8- μm CMOS processes.

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