

# A Packaged 1.1-GHz CMOS VCO with Phase Noise of $-126$ dBc/Hz at a 600-kHz Offset

C.-M. Hung and Kenneth K. O

**Abstract**—A packaged 1.1-GHz CMOS voltage-controlled oscillator (VCO) with measured phase noise of  $-92$ ,  $-112$ , and  $-126$  dBc/Hz at 10-, 100-, and 600-kHz offsets is demonstrated. According to [1], these satisfy the GSM requirements. The extrapolated phase noise at a 3-MHz offset is  $-140$  dBc/Hz. The power consumption is 6.8 and 12.7 mW at  $V_{DD} = 1.5$  and 2.7 V, respectively. The VCO is implemented in a low-cost 0.8- $\mu$ m foundry CMOS process, which uses p+ substrates with a p-epitaxial layer. Buried channel PMOS transistors are exclusively used for lower  $1/f$  noise. The inductors for the LC tanks are implemented using a series combination of an on-chip spiral inductor, four bond wires, and two package leads to increase  $Q$ . This technique requires no extra board space beyond that needed for the additional package leads.

**Index Terms**—Bond wires, CMOS, high- $Q$  inductor,  $1/f$  noise, package, RF, voltage-controlled oscillator.

## I. INTRODUCTION

**S**ATISFYING the GSM phase noise requirement for a CMOS voltage-controlled oscillator (VCO) [1] has been a major challenge. To present, the 1-GHz CMOS VCO with the lowest reported phase noise performance is the one implemented in a 0.8- $\mu$ m CMOS process with phase noise of  $-125$  and  $-137$  dBc/Hz at 600-kHz and 3-MHz offsets [2]. This VCO unfortunately consumes 66 mW of power at  $V_{DD} = 3$  V, which is high. In this paper, a packaged 1.1-GHz CMOS VCO that consumes only 12.7 and 6.8 mW of power at  $V_{DD} = 2.7$  and 1.5 V, and achieves superior phase noise performance, is reported. The VCO is fabricated in a low-cost 5-V, 0.8- $\mu$ m foundry CMOS process with three metal layers and is mounted in a silicon-on-insulator-like test package. The process uses a p+ substrate with a p- epitaxial layer, and this exacerbated the low- $Q$  factor problem of on-chip inductors [3]. To overcome this limitation, the inductor of the LC resonator is formed using a series combination of an on-chip patterned-ground-shield (PGS) [4] spiral inductor and bond wire and package lead inductances. This approach does not require extra board space. The VCO exclusively uses buried channel PMOS transistors for lower  $1/f$  noise [2].

## II. INDUCTOR DESIGN

This VCO uses the same schematic (Fig. 1) as the previously reported VCO [2]. The major design difference is the way in

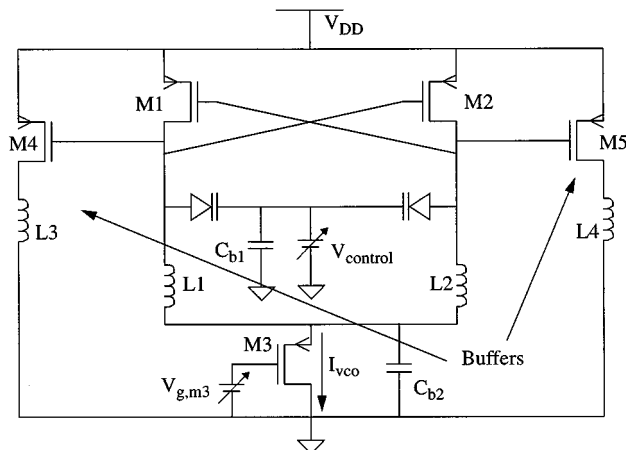


Fig. 1. A circuit schematic of the LC oscillator including buffers. The VCO exclusively uses buried channel PMOS transistors with low  $1/f$  noise for improved phase noise performance.

which the inductors for the LC tanks are implemented. In this work, the inductors are implemented using a series combination of a PGS inductor [4], four bond wires, and two package leads in order to increase  $Q$ . This lowers the power consumption and phase noise. Fig. 2 shows a bonding diagram for the chip and associated inductances. Leads 3 and 4 and leads 5 and 6 are connected in series with an external interconnect. As seen in Fig. 2, this interconnect does not increase the board space beyond the area requirement for additional leads nor the number of components mounted on the board since the interconnect can be directly printed on the board. The inductor was optimized using  $Q$  factors estimated with the half-bandwidth method [5], [6]. Inductances  $L1$  and  $L2$  were chosen to be  $\sim 7.1$  nH. A concern for using this type of inductor is the inductance variation due to the variability of the length of bond wires and the position of shorting wires relative to the leads, which could result in mismatches between  $L1$  and  $L2$  and could detune the center frequency  $\omega_0$ . To reduce this effect, a 2.1-nH ( $\sim 30\%$  of  $L1$  and  $L2$ ) PGS inductor is used as a part of the inductors. Additionally, double bond wires are used for each path between the lead and chip to reduce their inductance contribution, thus reducing the variation of the total inductance. Because of these, the variability in this approach should be smaller than those in the other VCO works using only bond wires [7], [8].

Taking the self- and mutual inductances of bond wires ( $L_{b1}-L_{b4}$ ) (Fig. 2) into account, the total bond-wire inductance  $L_{b, \text{tot}} = (L_{b1} \cdot L_{b2}) / (L_{b1} + L_{b2}) + (L_{b3} \cdot L_{b4}) / (L_{b3} + L_{b4}) + L_M$  where  $L_M$  is the total mutual inductance and is  $L_{m, (b1, b2)} + L_{m, (b3, b4)} - L_{m, (b1, b3)} - L_{m, (b1, b4)} - L_{m, (b2, b3)} - L_{m, (b2, b4)}$ .  $L_{m, (a, b)}$  in the above represents the mutual inductance between  $L_a$  and  $L_b$ . Similarly, the total lead inductance

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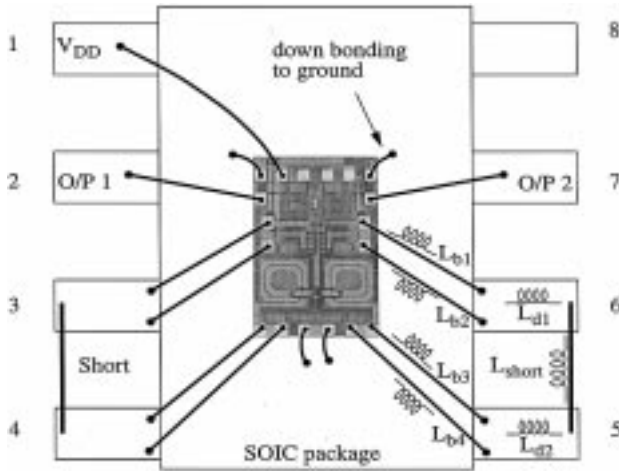


Fig. 2. A bonding diagram for packaging the VCO. The inductor for the LC tank utilizes a series combination of a short, two leads, four bond wires, and an on-chip spiral inductor. The parasitic series resistances and shunt capacitances are not shown in the model.

$L_{d,tot} = L_{d1} + L_{d2} - L_{m,(d1,d2)}$ . The computed  $L_{b,tot}$  and  $L_{d,tot}$  are 1 and 2.71 nH, respectively. Assuming that the mutual inductances between the short and bond wires are negligible, the short contributes  $\sim 1.2$  nH to the total. For the 2.1-nH PGS inductors, shunted metal 2 and 3 layers are used for the inductor trace, and a polysilicon layer is used for the ground shield. The area of the inductor is  $300 \times 300 \mu\text{m}^2$ . The metal spacing and width and number of turns are 2, 36, and 2.25  $\mu\text{m}$ , respectively. The parasitic capacitance seen looking into the PGS inductor is  $\sim 0.95$  pF. In an attempt to examine the variability of the bond wire inductance and the position of the shorting wires, three VCO's were packaged manually, and their tuned frequency at  $V_{DD} = 2.7$  V and power consumption of 12.7 mW has been measured. The tuned frequency ranged between 1.087 and 1.097 GHz ( $\sim 1\%$ ). This corresponds to  $\sim 1.8\%$  variation of the total inductance. Through a simulation study, the maximum mismatch between L1 and L2 for avoiding the second resonance [9] is 1.71 nH (24%). The observed variability is well below the tolerable inductance variation. If the VCO's are packaged using automated equipment, the variability should be even smaller. Because of the limited number of samples, it is not possible to conclude that the variation is not a problem. At the same time, a large variability is not observed.

The PGS inductor was designed neglecting the substrate effects [4]. To shield the magnetic field from the  $p^+$  substrate, eddy current should be induced in the ground shield. However, since the PGS is specifically designed so that eddy current is not induced, the PGS is not effective in reducing the eddy current effects in the  $p^+$  substrate. Thus, the actual  $Q$  and inductance of the spiral inductor are not as high as the design values. The spiral inductor design should have included the substrate effects. The  $Q$  of the total inductor including the on-chip inductor, leads, bond wires, and short connection was estimated to be  $\sim 17$  at 1.1 GHz (neglecting the substrate effects). This in a combination with the lower  $1/f$  noise of the buried channel PMOS transistors has led to the low measured phase noise at low power.

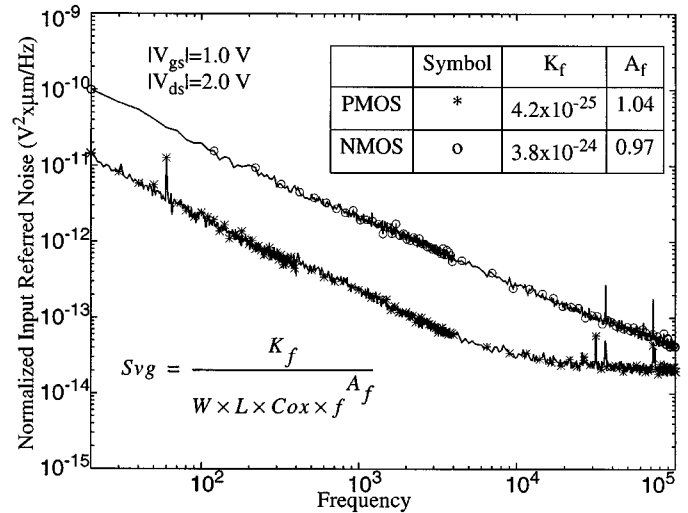


Fig. 3. Noise spectra of a PMOS and an NMOS transistor at  $|V_{GS}| = 1.0$  V and  $|V_{DS}| = 2.0$  V.

### III. AMPLIFIER AND VARACTOR DESIGN

Fig. 3 shows normalized (to 1- $\mu\text{m}$  channel width) input-referred  $1/f$  noise spectra for NMOS and buried channel PMOS transistors from the 0.8- $\mu\text{m}$  CMOS process. The PMOS flicker noise is around one order of magnitude lower than that of the NMOS noise. If the dc bias current were kept the same for the transistors by adjusting the widths, the difference would have been even greater. Hence, buried channel PMOS transistors were exclusively used in the VCO.

The  $g_m$  of the cross-coupled transistors M1 and M2 was chosen to be approximately four times higher than that required for critical oscillation in order to increase the signal level at the output. Instead of an NMOS current source, a PMOS transistor M3 is placed at the bottom to perform a comparable function. This configuration allows the VCO core output to be dc coupled to the buffer while maintaining the flexibility for setting the gate bias voltage of the buffer transistors (M4 and M5) without using an NMOS transistor with higher  $1/f$  noise. A high- $Q$  [10] capacitor  $C_{b2}$  is connected in parallel with M3 to reduce the ripple at its source, which could result in FM noise at the VCO outputs. The output of the VCO core has lower sensitivity to the noise at the gate of M3 (a source follower with a lower gain) compared to the topology with a conventional NMOS current source at the bottom, which is essentially a common-source amplifier with a higher gain. This lower sensitivity reduces the fluctuations of the tail current and the junction voltage and junction capacitance of the tuning diodes. Hence, the AM and FM noise at the VCO outputs can be reduced. The buffer is a PMOS common-source amplifier with an inductive load (13 nH), which can provide a larger and more symmetric swing to the 50- $\Omega$  load than that from a resistively loaded buffer. The output dc level is 0 V, so that the output signal can be directly connected to a spectrum analyzer.

The transistors M1 and M2 are laid out in such a way as to reduce the substrate resistances for the gate-to-body ( $C_{gb}$ ) and drain-to-body ( $C_{db}$ ) capacitances in order to improve the  $Q$  of the overall resonator. The area of the transistors is reduced

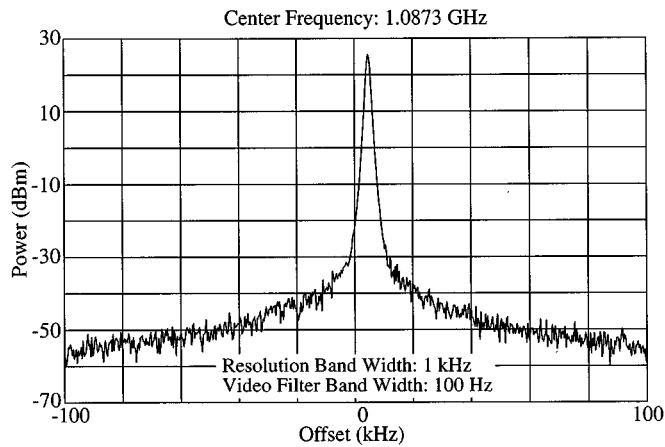


Fig. 4. A 200-kHz span output spectrum ( $I_{VCO} = 4.7$  mA,  $V_{DD} = 2.7$  V, and  $V_{control} = 2.7$  V). The power at the 1.09-GHz center frequency is +25.34 dBm. The phase noise at 10- and 100-kHz offsets are -92 and -112 dBc/Hz.

by eliminating the contacts of the source diffusions, which are shorted to n-well ties using a silicide layer. The  $Q$  factor for  $C_{db}$  at 1.1 GHz is  $\sim 57$ . The varactor is implemented using an array of p<sup>+</sup>-to-n-well diodes, and the capacitance is controlled by varying the n-well voltage. The n-well node is bypassed to ground using a 20-pF MOS capacitor ( $C_{b1}$ ) [10]. The measured  $Q$  of the varactor at 0-V bias and 1.1 GHz is  $\sim 24$ .

#### IV. EXPERIMENTS AND DISCUSSIONS

The phase noise was measured using an HP 8563E spectrum analyzer. The analyzer has a noise floor of -102 dBm for measurements with a resolution bandwidth (RBW) of 10 kHz. If the output power from the VCO is -17 dBm, the side band at a 600-kHz offset is very close to the noise floor, and the measurement of this side band is not very reliable. To improve the measurement accuracy, an external amplifier is connected at the output of the VCO. The amplifier has a gain of 42 dB, a noise figure of  $\sim 0.8$  dB, and a  $P_{1dB}$  of +26 dBm. Fig. 4 shows a single-ended output spectrum with a 200-kHz span and an RBW of 1 kHz.  $V_{DD}$ ,  $V_{control}$ , and  $I_{VCO}$  (Fig. 1) are 2.7 V, 2.7 V, and 4.7 mA, respectively. The signal power at the 1.09-GHz center frequency is +25.34 dBm, and the phase noise at 10- and 100-kHz offsets is -92 and -112 dBc/Hz, respectively. A phase noise plot up to the 600-kHz offset is shown in Fig. 5 (symbol "o"). The phase noise is -126 dBc/Hz at a 600-kHz offset, which exceeds the GSM requirement of less than -121 dBc/Hz [1] at this offset. The extrapolated phase noise at a 3-MHz offset assuming a slope of -20 dB/dec is -140 dBc/Hz. Oscillation frequency versus control voltage plot is shown in Fig. 6 (symbol "o"). The tuning range is  $\sim 103.7$  MHz for control voltages between 1.085 and 3 V and is 125.7 MHz if the control voltage range is extended to 5 V. Over these frequency ranges, the GSM phase noise requirements are satisfied. For control voltages lower than 1.085 V, the VCO still oscillates but the phase noise is too high to be used for GSM applications. When control voltages are below  $\sim 1.1$  V, the junction capacitance becomes high and the tuning diodes are turned on for a large portion of a period. These decrease  $Q$  of the tuning diode and internal signal level, leading to an increase of the phase

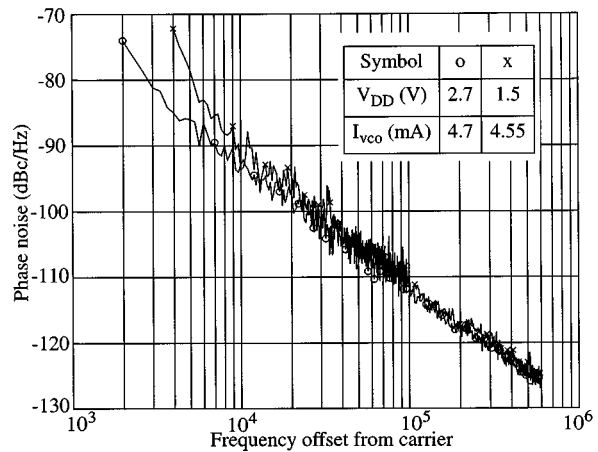


Fig. 5. The phase noise at 10- and 600-kHz offsets is -92 and -126 dBc/Hz, respectively, when  $V_{DD} = 2.7$  V and  $I_{VCO} = 4.7$  mA (symbol "o"), and -90 and -125 dBc/Hz, respectively, at  $V_{DD} = 1.5$  V and  $I_{VCO} = 4.55$  mA (symbol "x"). These exceed the GSM requirements of less than -85.4 and -121 [1] dBc/Hz, respectively.

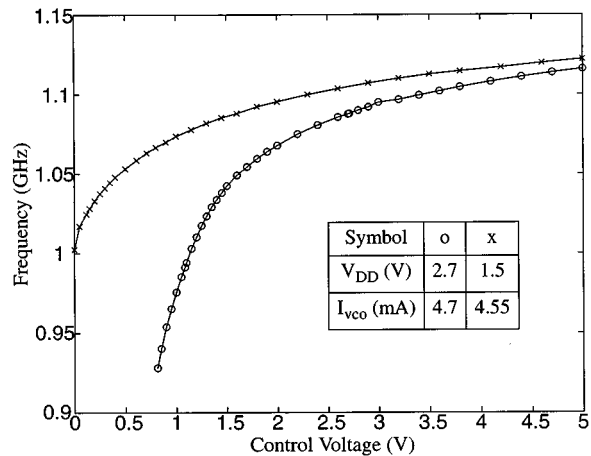


Fig. 6. Oscillation frequency versus control voltage plots. The tuning range at  $V_{DD} = 2.7$  V and  $I_{VCO} = 4.7$  mA (symbol "o") is 103.7 MHz for control voltages between 1.085 and 3 V and is 125.7 MHz if the control voltage range is extended to 5 V. At  $V_{DD} = 1.5$  V and  $I_{VCO} = 4.55$  mA (symbol "x"), the tuning range is 61.6 MHz for control voltages between 0.12 and 1.5 V and is 83.4 and 97.4 MHz if the voltage range is extended to 3 and 5 V, respectively. Over these frequency ranges, the GSM phase noise requirements are satisfied. At control voltages below the mentioned lower limits, the VCO still oscillates but the phase noise is too high for GSM applications.

noise. Increasing the current for the VCO core above 4.7 mA does not significantly reduce the phase noise since the internal voltage swing is near its maximum. However, the tuning range limited by the phase noise specification can be increased at the low-frequency side due to larger  $g_m$ , which increases the internal signal level at these frequencies.

The VCO core also works at 1.5-V  $V_{DD}$ . The phase noise plot is shown in Fig. 5 (symbol "x"). The center frequency is 1.09 GHz when both  $V_{DD}$  and  $V_{control}$  are 1.5 V and  $I_{VCO}$  is 4.55 mA ( $\sim 6.8$  mW). The phase noise at a 600-kHz offset is -125 dBc/Hz and is -139 dBc/Hz if extrapolated to a 3-MHz offset. The tuning range is 61.6 MHz for control voltages between 0.12 and 1.5 V and is 83.4 and 97.4 MHz if the control voltage range is extended to 3 and 5 V, respectively (Fig. 6, symbol "x"). The phase noise at a 600-kHz offset is less than -121 dBc/Hz within

these tuning ranges. At 1.5-V  $V_{DD}$ , due to a lower dc voltage at the drains of M1 and M2, the capacitance of the tuning diode at the same control voltage is smaller than that when  $V_{DD}$  is 2.7 V. This results in a higher oscillation frequency at a given control voltage.

The die photograph of the VCO is also shown in Fig. 2. The die size is  $1.2 \times 0.8 \text{ mm}^2$ . A significant portion of the die is occupied by the spiral inductors. All bond pads have a polysilicon ground shield underneath to reduce the substrate effect [11]. Empty space in the circuit layout is filled in with  $p^+$ -substrate contacts to reduce the substrate coupling while not forming any closed loops around the inductors.

## V. SUMMARY

A 1.1-GHz packaged VCO that exceeds the GSM phase noise requirement [1] has been demonstrated in a low-cost 0.8- $\mu\text{m}$  foundry CMOS process. The tank inductor is formed using a combination of a PGS inductor, bond wires, and package leads, and the VCO requires no extra board space beyond that required for additional package leads. The VCO core consumes 6.8 mW from a 1.5-V power supply and has a tuning range of 83.4 MHz for control voltages between 0.12 and 3 V. When  $V_{DD} = 2.7 \text{ V}$ , the VCO consumes 12.7 mW. The phase noise is  $-92$ ,  $-112$ , and  $-126 \text{ dBc/Hz}$  at 10-, 100-, and 600-kHz offsets, respectively, and the tuning range is 103.7 MHz for control voltages between 1.085 and 3 V. The low close-in phase noise was obtained by utilizing buried channel PMOS devices with low  $1/f$  noise and by using the package parasitics as part of the inductors to improve the  $Q$  of the LC resonators. The power consumption and phase noise of the VCO is comparable to those fabricated using Si-bipolar process technologies [12], [13].

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