Briefs

Body Bias Dependence of $1/f$ Noise in NMOS Transistors from Deep-Subthreshold to Strong Inversion

Namkyu Park and Kenneth K. O

***Abstract*—Dependence of $1/f$ noise on the body-to-source junction bias voltages (V_{BS}) between −2.5 and 0.5 V for 0.25-μm NMOS transistors is reported. In subthreshold, $1/f$ noise is reduced by about one order of magnitude when the body-to-source junction is forward biased by 0.5 V (V_{BS}) compared to that for $V_{\mathrm{BS}} = 0$ V, which is due to increased depletion layer capacitance as well as possibly due to an increased average distance between oxide traps and carriers by the forward bias. On the contrary, in strong inversion, $1/f$ noise remains almost constant for the entire V_{BS} range.**

I. INTRODUCTION

Low frequency noise of MOSFET's has been extensively studied. Based on the Hooge's mobility fluctuation model [1], [2], and McWhorter's number fluctuation model [3], [4], the dependences of MOSFET $1/f$ noise on bias [5]–[10], geometry [11], [12], process [13], and temperature [14] have been studied. Among the studies for bias dependence, the gate and drain bias dependences have been widely studied, while the body bias dependence of $1/f$ noise has been less extensively investigated. In particular, the effects of forward biasing body-to-source junction on $1/f$ noise of MOSFETs have not been previously investigated. This brief reports that $1/f$ noise of NMOS transistors can be significantly lowered in the subthreshold region by slightly forward-biasing the body-to-source junctions. This observation can be partially explained by a model based on the number fluctuation theory [3], [7]. In light of recent speed improvement of MOS transistors, which has opened up the possibility of exploiting the exponential characteristics of subthreshold operation in a wider range of analog circuits, this is unexpected good news. This can be used in triple-well analog CMOS technologies with isolated p-wells, which are being adopted to reduce the impact of substrate noise in mixed signal ICs [15], to decrease soft error rate (SER) in a DRAM [16], and to improve latch-up immunity [17].

II. EXPERIMENT

The noise and dc parameters were measured using NMOS transistors with a channel width, an effective channel length, and a gate oxide thickness of 300 μm, 0.25 μm, and 5 nm, respectively. First, the transistors were measured at V_{GT} (V_{GS}–V_{TH}) of −0.2, −0.1, 0, and 0.3 when the body-to-source voltage (V_{BS}) is 0 V. The corresponding drain-to-source currents (I_{DS}) are 4 μA, 60 μA, 500 μA, and 10 mA, respectively. The drain-to-source voltage (V_{DS}) was 1 V. Using these as the starting point, V_{BS} was varied between −2.5 to 0.5 V and $1/f$ noise was measured on wafer and compared at constant current. Because changing V_{BS} modifies the threshold voltage (V_{TH}), V_{GS} was adjusted to keep the current constant or to maintain the degree of inversion approximately the same. Keeping the current constant is also meaningful from the circuit design point of view, since performance of analog circuits are commonly compared at a given level of power consumption or dc bias current.

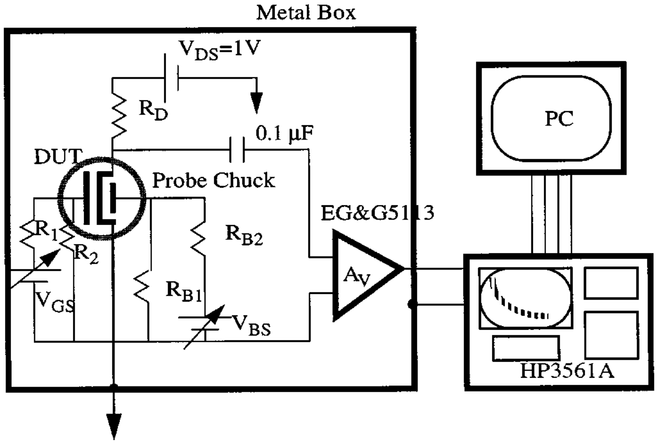

Fig. 1. $1/f$ noise measurement setup on wafer level.

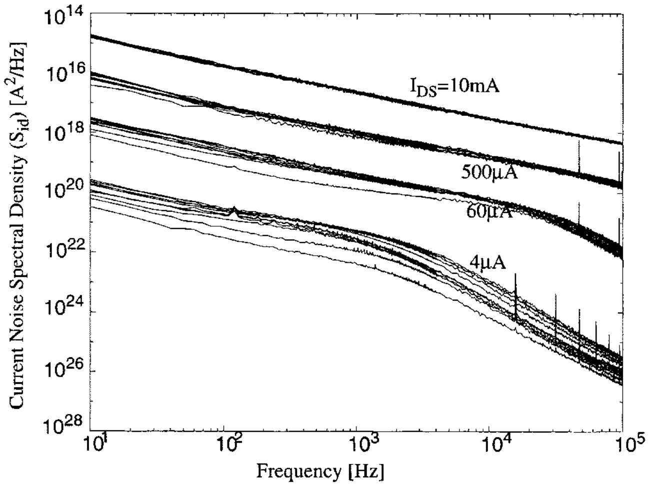

Fig. 2. Drain current noise power spectral density (S_{id}) for NMOS (300 μm/0.25 μm) at varying inversion conditions ($V_{\mathrm{GS}} - V_{\mathrm{TH}}$) and body-to-source bias (V_{BS}) in saturation region ($V_{\mathrm{DS}} = 1$ V).

Noise at the drain is amplified by a preamplifier (EG&G 5113) and measured using an HP3561A Dynamic Spectrum Analyzer (DSA). The measurement set up was kept in a shielded metal box except the DSA and a computer, as shown in Fig. 1. DC parameters such as $I_{\mathrm{DS}}, g_m, g_{\mathrm{ds}}, V_{\mathrm{TH}}$, and subthreshold slope (S) were measured using an HP4155. Threshold voltage (V_{TH}) was 0.51 V at $V_{\mathrm{BS}} = 0$ V. Changing V_{BS} from −2.5 to 0.5 V decreases V_{TH} from 0.91 to 0.35 V and increases S from 78 to 110 mV/decade.

III. RESULTS AND DISCUSSION

Fig. 2 shows the current noise at drain for all the measurement conditions. At high frequencies, the frequency dependence deviates from

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The authors are with the Department of Electrical and Computer Engineering, Silicon Microwave Integrated Circuits and Systems Research Group (SiMICS), University of Florida, Gainesville, FL 32611 USA.

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$1/f$ due to the gain roll-off associated with the low pass filter action of the effective resistance and capacitance of the MOSFET and preamplifier. This problem is particularly prominent when $V_{\rm GT}$ is small because the effective resistance of the MOSFET is high. Fig. 3 shows the $V_{\rm BS}$ dependence of $1/f$ noise at 1 kHz for different inversion conditions. In subthreshold, the noise is reduced by an order of magnitude when the body-to- source junction is forward-biased. The noise reduction becomes smaller as the silicon surface is more strongly inverted. At $V_{\rm GT} = 0$ V, the noise is reduced by around 50%. A concern for the noise analysis with the forward biased body-to-source junction is the impact of the parasitic bipolar action. When a body-to-source junction (base-emitter junction for the parasitic BJT) is forward biased by +0.5 V, the body-to-source junction current ($I_{\rm BS}$) or base current is 10 nA. The current gain of the parasitic BJT ($\beta_{\rm BJT}$) is 1 at $V_{\rm DS} = 1$ V and $V_{\rm BS} = 0.5$ V (maximum $\beta_{\rm BJT} = 4.5$). Hence, the collector current of BJT ($I_C = I_{\rm BS} \times \beta_{\rm BJT}$) is negligibly small (~10 nA) compared to the lowest fixed drain current of 4 μA. Clearly, these small bipolar currents cannot be the reason for the noise reduction of one order.

The current noise power spectral density at drain is given by (1) [7]

$$S_{\rm id} = \frac{I_{\rm DS}^2 q^4 \lambda N_t}{L^2 W k T f^\gamma} \int_0^L \frac{1}{(C_{\rm OX} + C_D + C_{\rm IT} - Q_n/V_T)^2}\, dy \quad (1)$$

where

V_T	thermal voltage (kT/q);
k	Boltzmann's constant;
q	$= 1.6 \times 10^{-16}$C;
λ	tunneling constant for electron;
T	absolute temperature;
$C_{\rm OX}$, C_D, $C_{\rm IT}$	oxide, depletion, and interface charge capacitance per unit area, respectively;
N_t, Q_n	trap and inversion carrier density per unit area;
L	effective channel length;
γ	exponent ranging from 0.8 to 1.2.

Equation (1) can be used to partially explain the $V_{\rm BS}$ dependence of $1/f$ noise from subthreshold to strong inversion. The denominator of the term inside the integral becomes $\sim(C_{\rm OX} + C_D + C_{\rm IT})^2$ in subthreshold, and $\sim(Q_n/V_T)^2$ in strong inversion [7]. In subthreshold, a positive body bias reduces the depletion layer width, which increases the depletion capacitance (C_D). When a number of trapped carriers fluctuates, increased C_D leads to an increased fluctuation of depletion charges. This leads to a decreased fluctuation of inversion carriers and current because of the charge conservation requirement [7]. This is reflected as the increase of C_D term in the denominator of (1), and as the decrease in $S_{\rm id}$ with increasing forward-bias in Fig. 3. Fig. 4 shows measured $S_{\rm id}$ and $C_{\rm dm}$ ($C_D + C_{\rm IT}$) and computed $S_{\rm id}$ using (1) at $I_{\rm DS} = 4$ μA. $S_{\rm id}$'s and $C_{\rm dm}$ were normalized with $S_{\rm id}$ and $C_{\rm dm}$ at $V_{\rm BS} = 0$ V, respectively.

This explanation can only partially explained the measurements. The measured noise drops around twice as fast as the computed noise using the measured $C_{\rm dm}$. This difference could be due to neglecting the position dependence of $C_{\rm dm}$ and Q_n in the noise computation, and due to an increase in the distance between oxide traps and free carriers caused by broadening of the inversion layer when the body-to-source junction is forward biased [19], [20], which decreases the trapping and detrapping rates. Once an inversion layer is formed, the fluctuation of trapped charges becomes dominated by the charge exchange with the inversion layer. Because of this, in strong inversion, the $V_{\rm BS}$ dependence of $1/f$ noise arising from the charge exchange with the depletion layer becomes weaker. In terms of (1), Q_n/V_T term becomes much larger than $C_{\rm IT}$, C_D, and $C_{\rm OX}$ in strong inversion, and changing $V_{\rm BS}$ or $C_{\rm IT} + C_D$ has almost negligible impact on $S_{\rm id}$ if Q_n ($\sim C_{\rm OX} V_{\rm GT}$) is kept approximately the same by keeping the current constant.

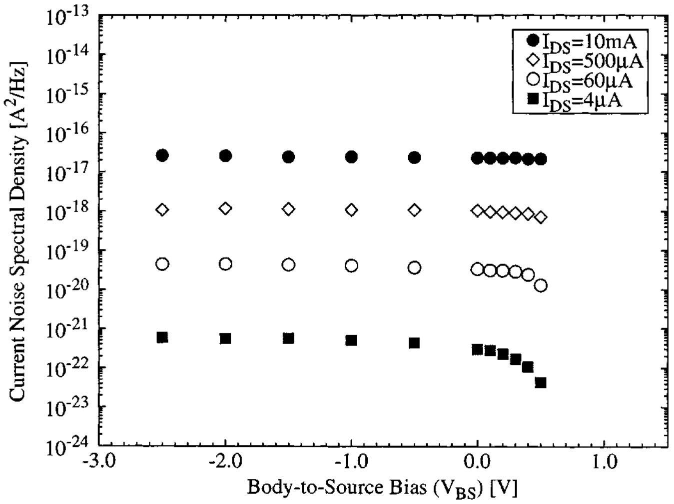

Fig. 3. Drain current noise power spectral density ($S_{\rm id}$) versus body-to-source bias ($V_{\rm BS}$) for NMOS (300 μm/0.25 μm) at 1 kHz under various inversion conditions with $V_{\rm DS} = 1$ V.

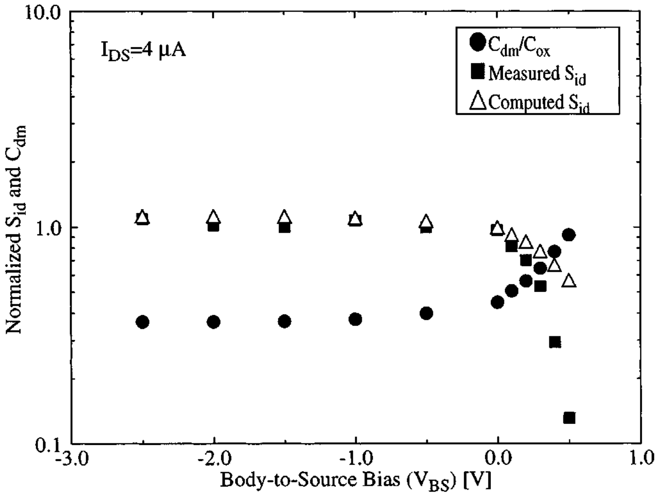

Fig. 4. Normalized drain current noise power spectral density ($S_{\rm id}$) and sum of depletion capacitance and interface state capacitance ($C_{\rm dm} = C_D + C_{\rm IT}$) for NMOS (300 μm/0.25 μm) [by $S_{\rm id}$ ($V_{\rm BS} = 0$ V) and $C_{\rm dm}$ ($V_{\rm BS} = 0$ V)] at $V_{\rm GT} = -0.2$ V and $V_{\rm DS} = 1$ V.

Possible problems associated with forward biasing the body-to-source junction are a voltage gain degradation at a given power consumption related to a reduction of $g_m/I_{\rm DS}$, increased latch-up susceptibility, and increased junction current and associated increases in power consumption and shot noise. It should be possible to effectively eliminate the latchup problem using triple well CMOS technologies [17] and using Schottky Clamped Drain MOS transistors [21]. For analog circuits with typically significant dc bias current, the effects of increased power consumption and shot noise due to the increased junction current can be made negligible by keeping the $V_{\rm BS}$ below 0.5 V.

In summary, an order of magnitude $1/f$ noise reduction is observed when the body-to-source junction for NMOS transistors is slightly forward biased in subthreshold. The noise reduction increases as the transistor is biased deeper into the subthreshold region. This is due to decreased depletion charges as well as possibly due to increased average distance between the Si/SiO$_2$ interface and free carriers. This noise reduction can be utilized to improve the low-frequency noise performance of analog circuits implemented in triple-well CMOS technologies [15]–[17].

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Effective Channel Length and External Series Resistance Models of Scaled LDD pMOSFETs Operating in a Bi-MOS Hybrid-Mode Environment

Siau Hing Lionel Seah, Kiat Seng Yeo, Jian Guo Ma, and
Manh Anh Do

***Abstract*—The effective channel length L_{eff} and total external series resistance R_{TOText} of deep submicron lightly doped drain (LDD) pMOSFETs, operating in a Bi-MOS hybrid-mode environment, have been modeled as functions of bias and temperature. The accuracy of the device threshold voltage used in the L_{eff} and R_{TOText} extraction routine is discussed. The proposed models have been verified for temperature ranging from 223 K to 398 K and source-to-body voltage $V_{\mathrm{SB}} \geq 0$ V conditions.**

***Index Terms*—Deep submicron, effective channel length, external series resistance, hybrid-mode, lightly doped drain (LDD), temperature-dependent.**

I. INTRODUCTION

The L_{eff} and R_{TOText} are important parameters needed to accurately model the I-V characteristics of short-channel LDD MOSFETs [1]. Most analyses in the literature (e.g., [2]–[12]) either ignore the body terminal of the devices, assume the body and source terminals having the same potential, or consider the source-body junction in reverse biased mode. Recently, hybrid-mode devices employing lateral p-n-p BJT in a pMOS structure have been brought into attention due to their high current gain and simple technology [13]–[15]. For a device operating in a Bi-MOS hybrid-mode environment, its gate and body terminals may be biased independently such that potential across the source-body junction becomes greater than 0 V, while maintaining the MOSFET in active mode. This requirement has prompted the question of whether or not L_{eff} and R_{TOText} commonly extracted from the experimental data remain valid for $V_{\mathrm{SB}} \geq 0$ V. The knowledge of such dependency on the body bias is important to ensure proper prediction of the device performance in hybrid-mode operation.

II. DEVICE STRUCTURES AND MEASURING EQUIPMENT

The device structure used in the measurement consists of a series of silicon p-channel LDD MOSFETs fabricated with a gate oxide thickness t_{ox} of 5 nm. The channel width W for all devices is 20 μm, whereas the gate length L varies from 1 μm down to 0.25 μm. N-well implantation was formed using phosphorus of 2×10^{13} cm^{-2} dosage and an energy level of 600 keV. The drain/source implantation was carried out using boron with a dose of 3×10^{15} cm^{-2} and an energy level of 30 keV. The p^{-} LDD implants were established with a dose of 2×10^{14} cm^{-2} and an energy level of 20 keV. The p^{+} junction depth X_j and the p-LDD junction depth r_j are approximately 0.15 μm and 0.075 μm, respectively. A channel implant dose of 3×10^{12} cm^{-2} and an energy level of 70 keV is added for threshold voltage adjustment. Device measurements were performed using a semiconductor parameter analyzer and a TEMPTRONIC system which controls the temperature of the wafer

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The authors are with the Division of Circuits and Systems, School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore 639798.

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