

Schottky Barrier Diodes for Millimeter Wave Detection in a Foundry CMOS Process*

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Abstract

CoSi₂-Si Schottky barrier diodes on an n-well and on a p-well/substrate are fabricated without a guard ring in a 130-nm foundry CMOS process. The n and p-type diodes with an area of 16 x 0.32 x 0.32 μm² achieve cut-off frequencies of ~1.5 and ~1.2 THz at 0-V bias, respectively. These are the highest cut-off frequencies for Schottky diodes fabricated in foundry silicon processes. The leakage currents at 1.0-V reverse bias vary between 0.4 to 10 nA for the n-type diodes. The break down voltage for these diodes is around 15 V. It should be possible to use these in millimeter wave and far infrared detection.

Index Terms: Schottky barrier diodes, cut-off frequency, silicon, and THz

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I. Introduction

Schottky barrier diodes due to their high operating frequencies and low forward voltage drop have been extensively studied and widely used [1],[2]. Their applications include RF signal rectification/detection, mixing and imaging [3]-[5]. Schottky diodes with cut-off frequencies up to 1 THz have been demonstrated on high-resistivity silicon substrates by growing a thin Molecular Beam Epitaxial layer on top of an n^+ layer [6],[7]. Schottky contacts have been realized by directly contacting an n-well with Aluminum metallization [8]. Schottky barriers have also been demonstrated by blocking n^+/p^+ implantation in selected diffusion regions [9],[10]. Using the latter approach, this paper reports CoSi_2 -Si Schottky diodes with extrapolated cut-off frequencies of $\sim 1.5/1.2$ THz. This by far is the highest cut-off frequency for Schottky diodes realized in foundry CMOS technologies. This work suggests new potential applications of CMOS technology in millimeter wave and far infrared detection.

II. Device Design and Layout

A cross-section and a layout of n and p-type Schottky diodes are shown in Figs.1(a) and (b). The ohmic contacts to the n/p-wells around the schottky contact form the second terminal. The cut-off frequency (f_{cutoff}) [2],[7] of Schottky diodes is given in Eq. (1).

$$f_{cutoff} = \frac{1}{2\pi \times R_s \times C_o} \quad (1)$$

The series resistance, R_s is due to the vertical resistance (R_1), the resistance associated with the well region under the shallow trench and well contact (R_2), and the contact/metal resistance (R_3). The capacitance, C_o is due the zero bias junction capacitance and parasitic interconnect capacitance. The individual resistances and capacitances that constitute R_s and C_o are also shown in Fig. 1(a).

The series resistance is reduced by minimizing the space between the Schottky contact and n^+/p^+ diffusion regions. R_s is further reduced by increasing the n^+/p^+ diffusion width and by having multiple contacts on the diffusion regions. The metal connections to Schottky and n^+/p^+ diffusions are spaced wide apart ($0.7 \mu\text{m}$) to reduce the sidewall parasitic capacitance. This is the key for achieving the cut-off frequency higher than 1 THz using the 130-nm CMOS process. Because the minimum diode area (A_s) and metal-to-metal spacings of 8 metal layers can be small, the impact

of parasitic capacitance can be particularly great. The only controllable parameter in the design of these diodes is the device cross-section area A_s , since all the other parameters are set by the process. Simple analyses show C_o to be proportional to A_s and R_s to be roughly proportional to $A_s^{-0.5}$, hence decreasing A_s increases the cutoff frequency. Because of this, the Schottky contact area (A_s) is set to the minimum contact diffusion area permitted by the process of $0.32 \times 0.32 \mu\text{m}^2$. Due to this small diode area, even with the $0.7\text{-}\mu\text{m}$ spacing, the metal-to-metal capacitance is $\sim 25\%$ of the total capacitance.

To improve the power handling capability and measurement accuracy, 16 Schottky-cells are connected in parallel. A straightforward computation [2],[11] predicted that C_o is ~ 7 fF and R_s is $\sim 10 \Omega$ for this array. It is important to limit the total capacitance value to make sure that R_s is sufficiently larger than the contact resistance of high frequency probes ($1\text{-}2 \Omega$). The structures were configured for one-port measurements. The ground shielded bond pads [11]-[13] with a reduced area of $50 \times 54 \mu\text{m}^2$ and capacitance of 28 fF are used to increase the device capacitance to de-embedded capacitance ratio once again to improve the measurement reliability. A short structure and a dedicated open structure for each of the diodes are used to de-embed the parasitic capacitances and resistances [11].

III. Measurement Results and Discussions

A. Junction Capacitance and Series Resistance Measurements/RF Characterization

The plots of extracted R_s and C_o for the n and p-type devices from the measured one-port S-parameters between 15 and 20 GHz using a Vector Network Analyzer (HP-8510C) are shown in Figs. 2(a) and (b). The capacitances are relatively constant over the frequency range. The resistances, however exhibit significant variations about a mean value. This is caused by the values of resistances and capacitances being simultaneously small and the de-embed capacitance being larger than the diode capacitance. The cut-off frequencies computed using Eq. (1) range between 1 to 3 THz (~ 1.5 THz average) for the n-type diode, and between 1 to 1.7 THz (~ 1.2 THz average) for the p-type. The n-type diode has a higher f_{cutoff} due to slightly lower capacitance. This may be due to the higher built-in potential of n-type devices. The plots of f_{cutoff} versus bias are shown in Fig. 3. For both of the devices, f_{cutoff} decreases with bias voltage due to the monotonic increase of C_o with bias. Surprisingly, the measured resistance and capacitance are in good agreement with

the simulated estimates. However, full 3-D EM simulations are needed to better understand particularly their behaviors at frequencies above 100 GHz.

B. I-V Measurements/DC Characterization

Fig. 4. shows the current density-voltage (J-V) curves for the n and p-type diodes. For both of these diodes, the current increases by a decade for ~ 65 -mV increase in forward bias which indicates an ideality factor of 1.08. The barrier heights of these devices computed using the Richardson-Dushman equation for the thermionic current [2] are ~ 0.35 eV for the p-type and ~ 0.52 eV for the n-type diodes. The turn-on voltages and forward knee currents (I_{KF}) are $\sim 0.4/0.3$ V and $\sim 1/0.6$ mA for the n and p-type structures, respectively. The reverse breakdown voltage is ~ 15 V for both of the devices with an appreciable reverse leakage current of $1 \mu\text{A}$ at ~ 10.5 V for the n-type and ~ 3 V for the p-type structures. The leakage current densities of n and p-type diodes at 1.0-V reverse bias vary between 0.02 and 0.6 A/cm^2 , and between 0.26 and 3.3 A/cm^2 , respectively. The actual leakage currents for the structures vary between 0.4 and 10 nA , and between 4.2 and 54 nA , respectively, which are not terribly high. This indicates that a guard ring for reducing the leakage current, which increases the capacitance and lowers the cutoff frequency may not be needed even for the 0-V dc bias operation. A possible reason for this pleasant surprise is the use of CoSi_2 - silicon junctions.

IV. Conclusions

Both n and p-type Schottky barrier diodes with cut-off frequencies of over 1 THz are realized in a 130-nm foundry CMOS process. No additional masks or modifications have been introduced to fabricate these devices. The excellent reverse bias characteristics circumvents the need of having guard ring structures to reduce the reverse leakage current. The high breakdown voltage suggests a potential use of these devices also in high power switches. The high cut-off frequencies indicate that these devices can very well be used for millimeter and infrared applications. This is more so when the technology node scales towards 65-nm and beyond, where cut-off frequency is expected to exceed 3 THz.

References

- [1] B. L. Sharma, *Metal-Semiconductor Schottky Barrier Junctions and Their Applications*. New York: Plenum, 1984.
- [2] M. Shur, *Physics of Semiconductor Devices*. NJ: Prentice Hall, 1990.
- [3] S. A. Maas, *Microwave Mixers*. MA: Artech House, 1986.
- [4] S. Mollenkopf and G.M. Rebeiz, "A 22 GHz MIC active receiver/radiometer," *IEEE MTT-S In. Microwave Symp. Dig.*, 1994, vol. 3, pp. 1347-1350.
- [5] N. Yutani, H. Yagi, M. Kimata, J. Nakanishi, S. Nagayoshi, and N. Tubouchi, "1040 x 1040 element PtSi Schottky-Barrier IR image sensor," *Int. Electron Devices and Millimeter Wave MIC*, Dec. 1991, pp. 175-178.
- [6] K. M. Strohm, J. Buechler, E. Kasper, J.F. Luy, and P. Russler, "Millimeter wave transmitter and receiver circuits on high resistivity silicon," *IEE Coll. in Microwave and Millimeter MIC*, Nov. 1988, no. 17, pp. 1-4.
- [7] K. M. Strohm, J. Buechler, and E. Kasper, "SIMMWIC Rectannas on High-Resistivity Silicon and CMOS Compatibility," *IEEE Transactions on Microwave Theory and Techniques*, May 1998, vol. 46, pp. 669-676.
- [8] V. Milanovic, M. Gaitan, J. C. Marshall, and M.E. Zaghoul, "CMOS Foundary Implementation of Schottky Diodes for RF Detection," *IEEE Transactions on Electron Devices*, Dec. 1996, vol. 43, no. 12, pp. 2210-2214.
- [9] F. J. Huang, K. K. O, "Metal-oxide semiconductor field-effect transistors using Schottky Barrier Drains (SBDR)," *IEEE Electron. Lett.*, 1997, vol. 33, pp. 2210-2214.
- [10] F. J. Huang, K. K. O, "Schottky-Clamped NMOS Transistors Implemented in a Conventional 0.8- μ m CMOS Process," *IEEE Electron. Lett.*, Sept. 1998, vol. 19, no. 9, pp. 326-328.
- [11] C. M. Hung, *Investigation of a Multi-GHz Single-Chip CMOS PLL Frequency Synthesizer for wireless applications*, Ph.D. Dissertation, University of Florida, 2000.
- [12] J. T. Colvin, S. S. Bhatia, K. K. O, "Effect of substrate resistances on LNA performance and a bondpad structure for reducing the effects in a silicon bipolar technology," *IEEE J. Solid-State Circuits*, Sept. 1999, vol. 34, pp.1339-1344.
- [13] T. E. Kolding, "Shield-based microwave on-wafer device measurements," *IEEE Microwave Theory and Tech.*, June 2001, vol. 49, pp. 1039-1044.

Fig. 1, (a) A cross section and individual components of R_s and C_o . (b) Layouts of n/p-type Schottky barrier diode cells.

Fig. 2, (a) R_s and C_o vs. frequency for n-type diodes. (b) R_s and C_o vs. frequency for p-type diodes.

Fig. 3, Average f_{cutoff} vs. bias voltage for n and p-type devices.

Fig. 4, Leakage current density vs. bias voltage for n and p-type diodes.

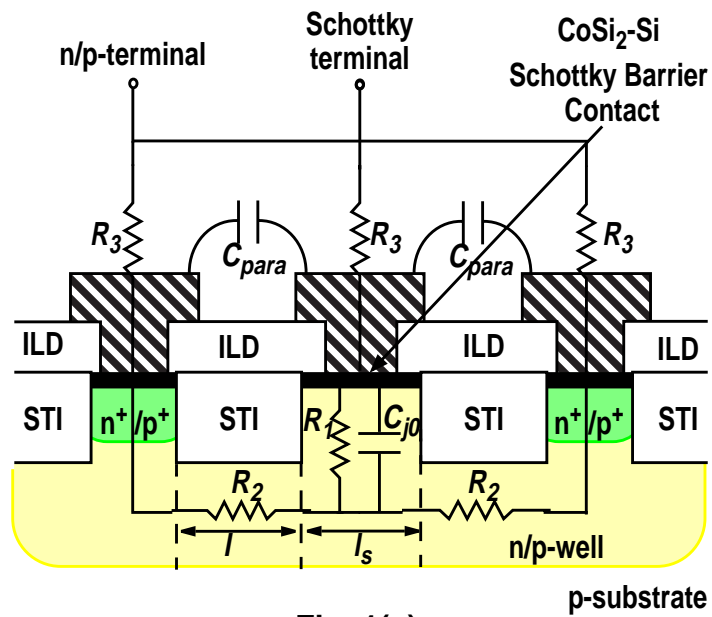


Fig. 1(a).

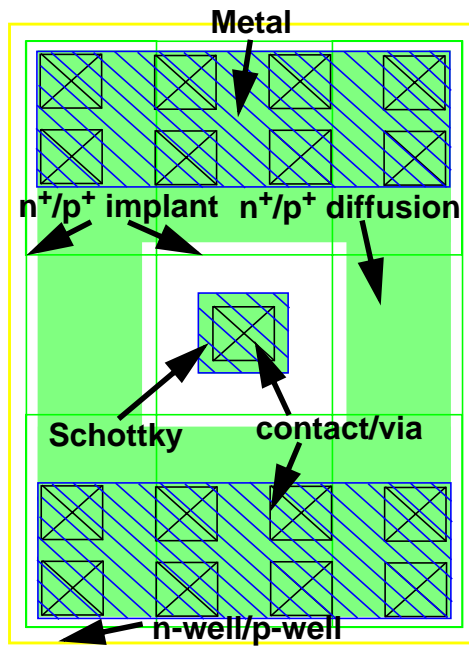


Fig. 1(b).

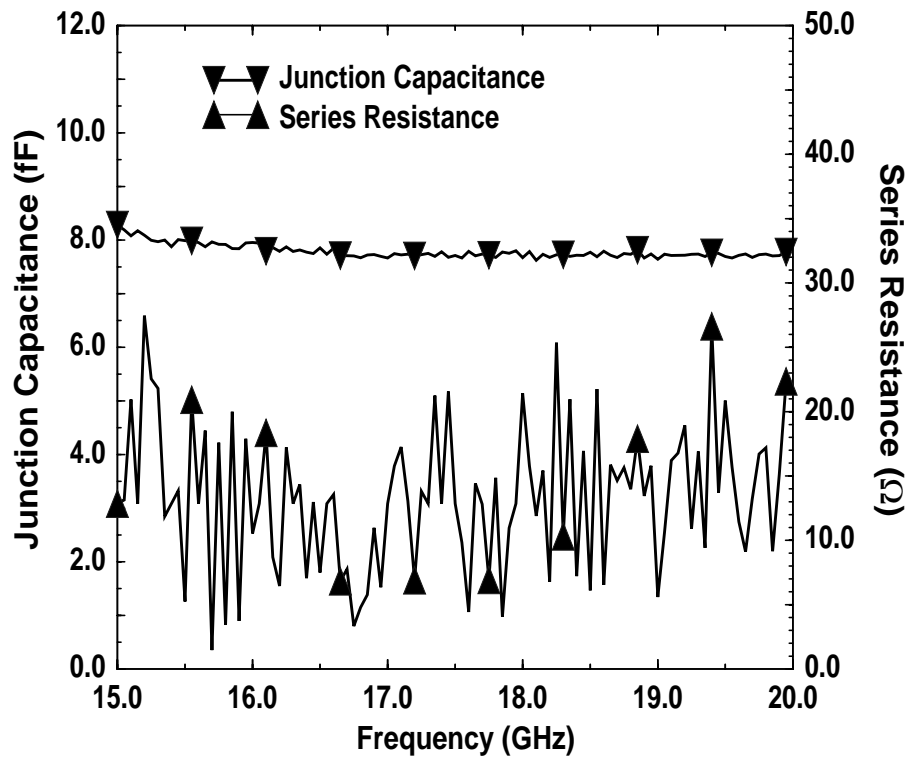


Fig. 2(a).

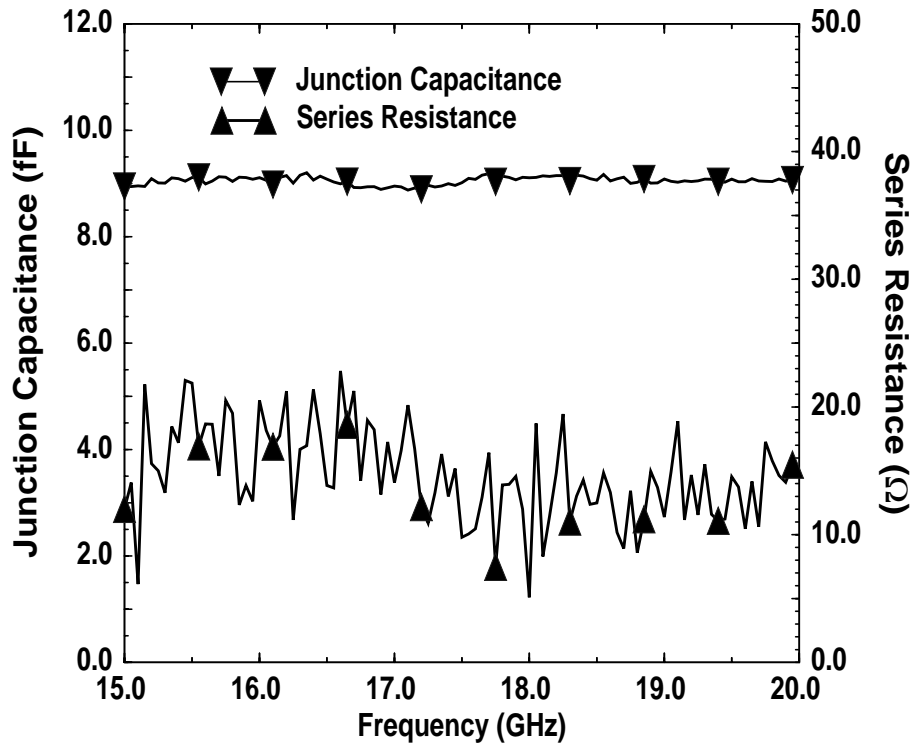


Fig. 2(b).

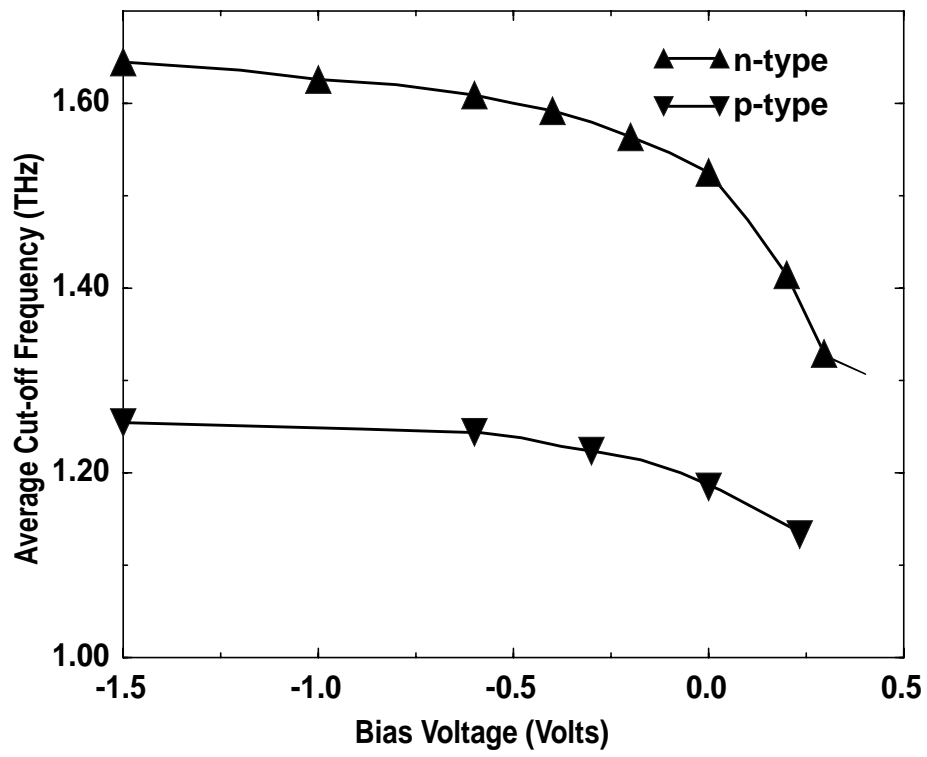


Fig. 3.

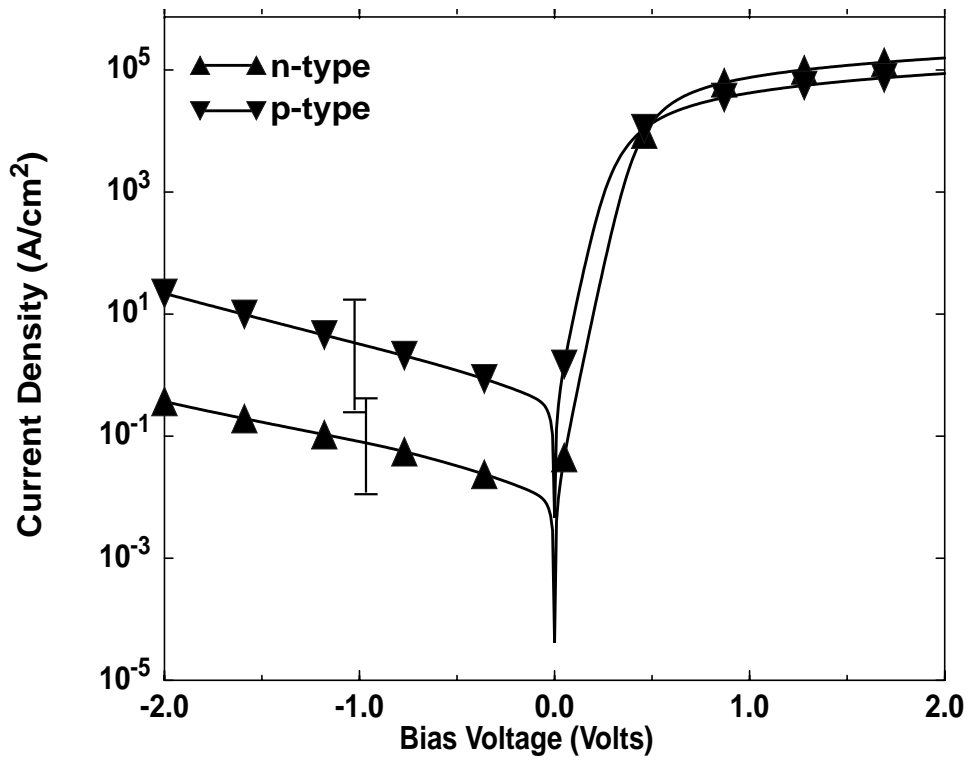


Fig. 4.