

A Schottky Diode with Cut-off Frequency of 400 GHz Fabricated in 0.18- μm CMOS

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TiSi₂-Si Schottky diodes for RF rectification were fabricated using a 0.18- μm CMOS process without any process modifications. These diodes are intended to be used with forward bias and small signal amplitude. At 0-V bias, the diodes with an area of $0.45 \times 0.45 \mu\text{m}^2$ achieve a cut-off frequency of over 400 GHz. This is the highest cut-off frequency compared to that for the previously reported Schottky diodes fabricated in foundry CMOS processes. The turn-on voltage of the diodes is $\sim 0.30\text{-V}$.

Indexing terms: Schottky diode, CMOS, and TiSi₂-Si

Introduction: Schottky barrier diodes due to their high operating frequencies and low forward voltage drop have been extensively studied and widely used [1],[2]. A Schottky barrier diode is a majority carrier device with improved high frequency capability owing to the absence of minority carrier storage. Their applications include RF signal rectification/detection and image sensing [3],[4]. Schottky barrier diodes with cut-off frequencies up to 1 THz have been demonstrated by depositing a layer of Ti-Pt-Au on a thin layer of n-type silicon grown on a n⁺ silicon layer using Molecular Beam Epitaxy (MBE) [5]. Schottky contacts have also been realized by introducing a direct contact between metal (Al-Si) and a moderately doped well in a CMOS process [6]. Addi-

tionally, Schottky diodes have been demonstrated using foundry Salicide CMOS processes [7],[8]. The diodes are implemented by blocking n^+/p^+ ion implantation in selected diffusion regions. This paper reports a Schottky diode implemented using the latter approach, with extrapolated cut-off frequency of over 400 GHz. The diode can be fabricated alongside the NMOS and PMOS transistors thus leading to lower cost and monolithic integration. This is the highest cut-off frequency reported to date for Schottky diodes realized in foundry silicon technologies.

Device Design and Layout: $TiSi_2$ -n-Si Schottky diodes have been fabricated by blocking n^+ implant in the diffusion region as shown in Fig. 1(a) [7],[8]. The ohmic contacts on n-well surrounding the Schottky contact form the second terminal. To reduce the series resistance (R_s), the spacing between the Schottky contact and n^+ region is kept at the minimum allowed by the process. The n^+ diffusion width is 1.2 μm which is large to reduce the n^+/n -well vertical resistance (R_3 in Fig. 1(b)). This also allows having multiple contacts on the n^+ diffusion region thus reducing the contact resistance associated with the n^+ terminal and hence R_s . Metal connections to the schottky and n^+ regions are spaced wide apart to reduce the sidewall capacitance between the two terminals. Fig. 1(b) shows the cross-section of device with the individual components that make up R_s and C_o . The cross-section includes the p^+ guard rings. The guard ring width is varied from 0.12 - 0.24 μm . The ratio of Schottky contact area to the p^+ guard ring area is fixed at ~ 3 . As will be demonstrated, having a guard ring decreases the leakage current. The devices without the guard ring are also fabricated. These devices has significantly smaller area and thus capacitance. The only controllable parameter in the design of these devices is the Schottky contact area (A_s), since all other parameters such as metal and semiconductor work functions are set by the process. Simple computational analyses have shown that the cut-off frequency (f_{cutoff}) in Eq.(1) [2] is a

monotonically decreasing function of A_s . Hence the contact area was set at the minimum value permitted by the process ($0.2024 \mu\text{m}^2$), which sets the length (l_s in Fig. 1(b)) to be around $0.45 \mu\text{m}$. In Eq.(1), R_s is the series resistance and C_o the diode capacitance at 0-V.

$$f_{cutoff} = \frac{1}{2\pi R_s C_o} \quad (1)$$

To improve measurement accuracy, 24 schottky-cells were connected in parallel. Since the device junction capacitance is smaller than the pad capacitance, new pads with reduced capacitance ($48 \times 48 \mu\text{m}^2$) using the top metal layer (metal 6) were utilized to reduce the measurement uncertainties resulting from this. To more accurately de-embed the unwanted parasitics, dedicated open structures for each diode were also fabricated and used [9]. A short structure is used to de-embed the probe contact resistance.

Measurement Results and Discussions: Fig. 2 shows the I-V curves of Schottky barrier devices with and without the p^+ guard rings. These devices have an ideality factor of ~ 1.8 which is large. For the $2.5 \times 2.5 \mu\text{m}^2$ diode without the guard ring, the reverse leakage current density at 1-V reverse bias is $\sim 44 \text{ A/cm}^2$. The barrier height of this device, computed using the Richardson-Dushman equation for the thermionic current [2] is $\sim 0.32 \text{ eV}$. For the device with a $0.18\text{-}\mu\text{m}$ wide p^+ guard ring and the same diffusion area ($2.32 \times 2.32 \mu\text{m}^2$ Schottky area), the reverse leakage current density drops down by a factor of ~ 100 at 1-V reverse bias and by a factor of ~ 6 at 3-V reverse bias. The guard rings also reduce the forward bias current by $\sim 3.5\text{X}$ at 0.35-V forward bias. The devices with p^+ guard rings show an abrupt change in current when the forward bias is larger than $\sim 2 \text{ V}$. This is caused by the p-n junction current becoming larger than the Schottky diode current. The diodes without the p^+ guard rings are leaky. This is a concern but it is a limita-

tion that can be tolerated if the devices are used in the forward bias region with limited voltage swing.

Fig. 3(a) shows the plots of series resistance and diode capacitance for a $0.45 \times 0.45 \mu\text{m}^2$ Schottky diode measured between 14 and 20 GHz using a Vector Network Analyzer (VNA). The capacitance and resistance are relatively constant over the frequency range. Using the measurement results at 20 GHz, the computed cut-off frequency (Eq. (1)) is over 400 GHz. The plot of cut-off frequency (f_{cutoff}) as a function of the bias is shown in Fig. 3(b). The cut-off frequency decreases with an increase of bias. This is due to the monotonic increase in diode capacitance with bias. The cut-off frequencies of the devices with the p^+ guard rings ($2.5 \times 2.5 \mu\text{m}^2$) are ~ 60 GHz or less. This reduction is due to the larger diffusion area resulting in a larger capacitance.

The resistance and capacitance of the 400-GHz diode turned out to be around twice the initial estimates. The series resistance turned out to be higher due to the higher sheet resistance of n-well under the shallow trench isolation (STI). Most of the additional measured capacitance can be attributed to the side-wall capacitance between the metal interconnects for Schottky and the n^+ contacts. If the parasitics are lowered, the cut-off frequency will be even higher. Scaling down the technology is also expected to yield a higher cut-off frequency due to the scaling down of area, sheet resistance of n-well and separation between the Schottky - n^+ contacts.

Conclusions: A Schottky barrier diode with a cut-off frequency of over 400 GHz is realized in a 0.18- μm foundry CMOS process. No additional masks or modifications have been introduced to fabricate the device. The TiSi_2 -Si Schottky barrier contacts were formed by blocking n^+ / p^+ implants in diffusion areas. The high leakage current is a concern, but this can be tolerated by using the devices in the forward bias region with limited voltage swing. Guard ringed structures

were fabricated by adding a p^+ implanted region surrounding the Schottky region. More than 100X reduction of reverse leakage current can be achieved by having a p^+ guard ring, however, this reduces the cut-off frequency by a factor of $\sim 6-7$. Lastly, this work has shown that the cut-off frequencies of Schottky diodes fabricated in foundry CMOS processes are sufficiently high for microwave and millimeter wave detection.

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Figure captions:

Fig. 1(a) A layout of the Schottky barrier cell.

Fig. 1(b) A cross section of Schottky barrier diode with p^+ guard ring. Structures with and without the guard ring have been fabricated.

Fig. 2 Current Density vs.voltage curves for the diodes with and without the guard rings.

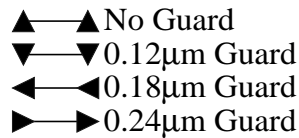


Fig. 3(a) Measured C_j and R_s for the array of 24 minimum geometry diodes connected in parallel.

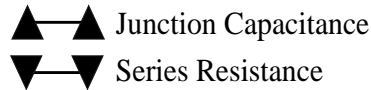


Fig. 3(b) f_{cutoff} as a function of bias voltage for the array of 24 minimum geometry diodes.

Figure 1(a)

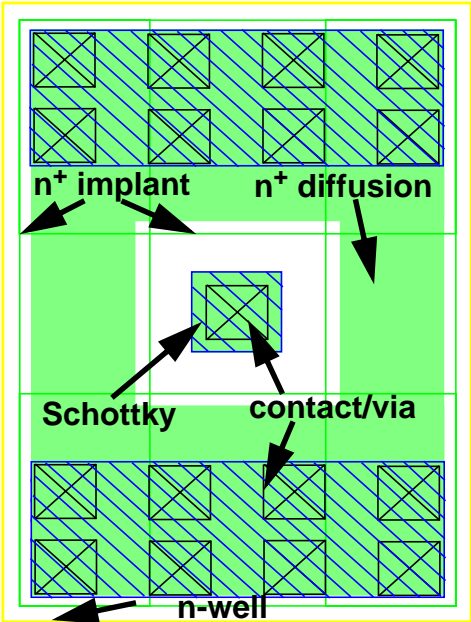


Figure 1(b)

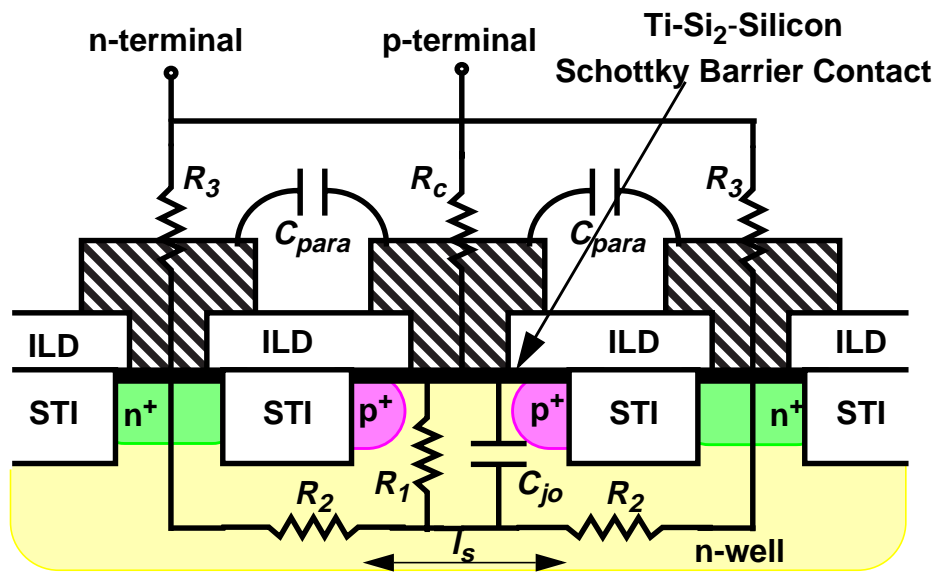


Figure 2

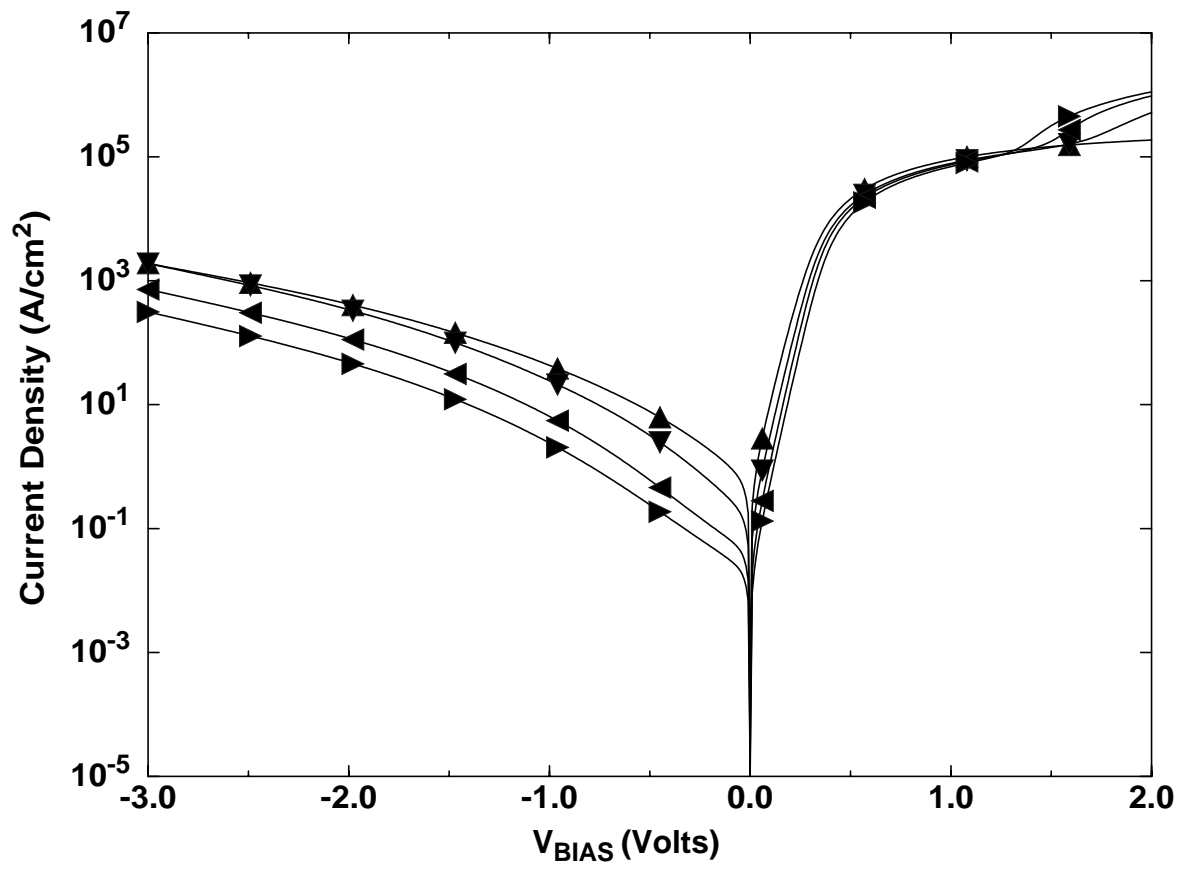


Figure 3(a)

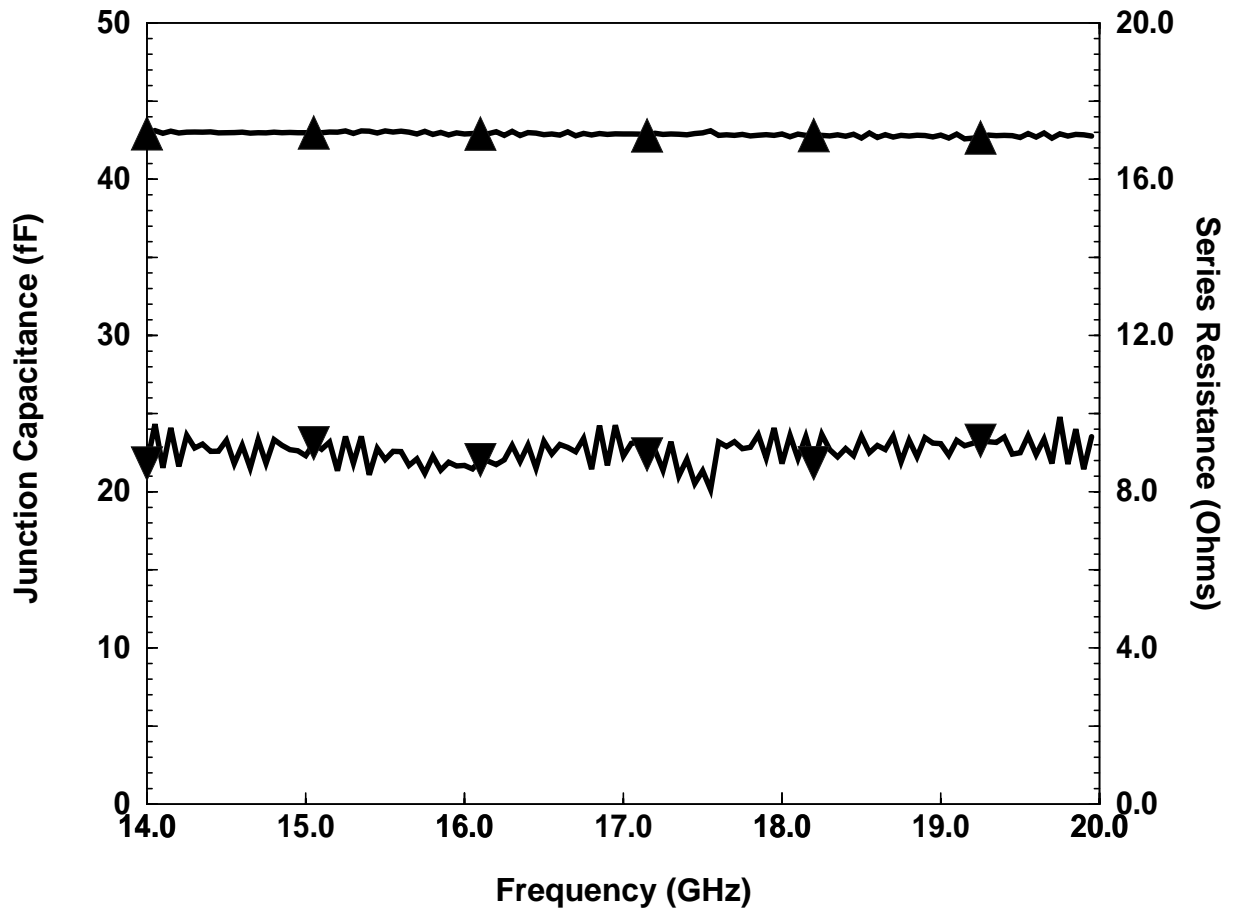


Figure 3(b)

